Actions ATJ2135N Product Datasheet

Latest Version: 1.0

May, 2008

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Revision History

Date	Revision	Description
May 2008	1.0	Initial version released;

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1 Introduction

Overview

The Actions ATJ2135N is a highly integrated 32bit RISC-based SoC for digital media solution. The RISC architecture and high speed bus controller are capable of achieving high performance with low power consumption. With a built-in JPEG co-processor, this media platform is capable of processing both JPEG and MJPEG format with higher efficiency. The integrated high-speed USB 2.0 SIE enables the platform to act as a mass storage device at the speed up to 480Mbps. The audio codec in the SoC is based on sigma-delta modulation, providing high performance with low power consumption as well as allowing the flexible adjustment of sample rates from 8k to 96k. The built-in audio codec is able to switch inputs within headphones, microphones, FM radios and direct drive for low impedance earphones.

The ATJ2135N also provides integrated SDRAM and Flash interfaces; IIC, IR and UART etc. interfaces for changeable control and transfer modes. The ATJ2135N therefore provides a true “ALL-IN-ONE” solution that is ideally suited for highly optimized digital media devices.

Features

- Audio playing support: WMA, OGG, APE, WAV, ASF, FLAC
- Audio recording support: WAV
- Video playing support: AMVB, XVID, WMV, FLV, MJPEG QVGA
- Image view support: JPEG, BMP, GIF, PNG
- High-speed USB 2.0 Device
- High Speed NAND I/F
- Supports SLC & MLC NAND FLASH with 8-bit Error Correction
- Supports SD/MMC FLASH Card
- OLED, TFT, STN support
- Integrated stereo DAC & ADC
- Li-Ion battery charger
- 11-16V backlight driver for LED
- 6bit battery monitoring ADC

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2 Pin Description

2.1 Pin Assignment

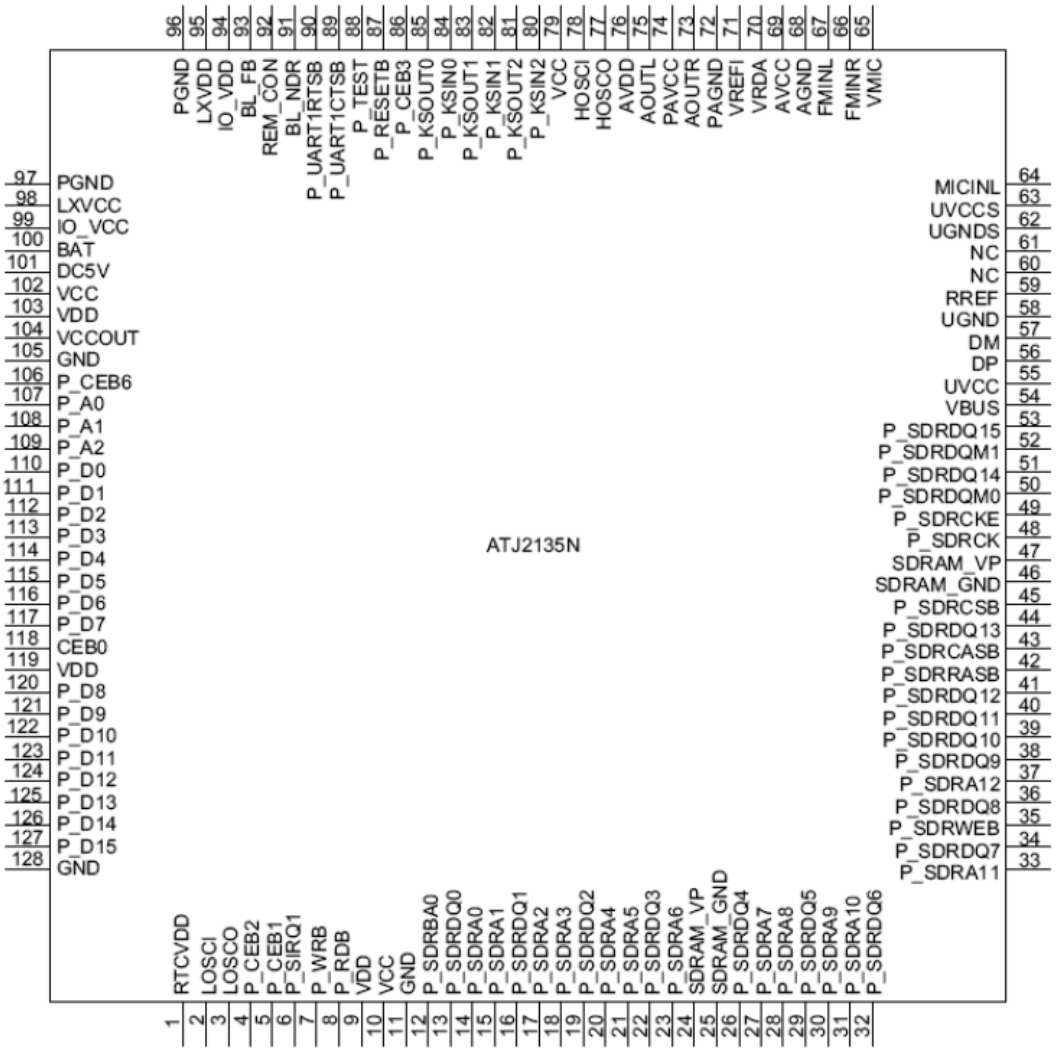

Figure 1: Pin Assignment

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2.2 Pin Definition

Table 1: ATJ2135N Pin Definition

Pin No.	Pin Name	Function Name	I/O Type	Reset Default	Short Description
1	RTCVDD	RTCVDD	PWRI		RTC Power VDD
2	LOSCI	LOSCI	AI		Low Oscillator Input
3	LOSCO	LOSCO	AO		Low Oscillator Output
4	CEB2	NF_CEB2 /RGB_CE	O	1	NAND FLASH Interface CE2 RGB Interface CE
		GPIOA17	BI		GPIOA Port 17
5	CEB1	NF_CEB1 /RGB_CE	O		NAND FLASH Interface CE1 RGB Interface CE
6	SIRQ1	SIRQ1	I	z	External IRQ 1
		GPIOB31	BI		GPIOB Port 31
7	WRB	NF_WR /RGB_WRB	O		NAND FLASH Interface WR RGB Interface WR
8	RDB	NF_RD /RGB_RDB	O		NAND FLASH Interface RD RGB Interface RD
9	VDD	VDD	PWRI		VDD
10	VCC	VCC	PWRI		VCC
11	GND	GND	PWR		GND
12	SDRBA0	SDRAM_BA0	O		SDRAM Interface Bank Address0
13	SDRDQ0	SDRAM_DQ0	BI		SDRAM Interface Data 0
14	SDRA0	SDRAM_A0	O		SDRAM Interface Address 0
15	SDRA1	SDRAM_A1	O		SDRAM Interface Address 1
16	SDRDQ1	SDRAM_DQ1	BI		SDRAM Interface Data 1
17	SDRA2	SDRAM_A2	O		SDRAM Interface Address2
18	SDRA3	SDRAM_A3	O		SDRAM Interface Address 3
19	SDRDQ2	SDRAM_DQ2	BI		SDRAM Interface Data 2

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20	SDRA4	SDRAM_A4	O		SDRAM Interface Address 4
21	SDRA5	SDRAM_A5	O		SDRAM Interface Address 5
22	SDRDQ3	SDRAM_DQ3	BI		SDRAM Interface Data 3
23	SDRA6	SDRAM_A6	O		SDRAM Interface Address 6
24	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
25	SDRGND	SDRAM_GND	PWR		SDRAM Interface GND
26	SDRDQ4	SDRAM_DQ4	BI		SDRAM Interface Data 4
27	SDRA7	SDRAM_A7	O		SDRAM Interface Address 7
28	SDRA8	SDRAM_A8	O		SDRAM Interface Address 8
29	SDRDQ5	SDRAM_DQ5	BI		SDRAM Interface Data 5
30	SDRA9	SDRAM_A9	O		SDRAM Interface Address 9
31	SDRA10	SDRAM_A10	O		SDRAM Address 10
32	SDRDQ6	SDRAM_DQ6	BI		SDRAM Interface Data 6
33	SDRA11	SDRAM_A11	O		SDRAM Interface Address11
		GPIOA25	BI		GPIOA Port 25
34	SDRDQ7	SDRAM_DQ7	BI		SDRAM Interface Data7
35	SDRWEB	SDRAM_WEB	O		SDRAM Interface Write Enable
36	SDRDQ8	SDRAM_DQ8	BI		SDRAM Interface Data 8
37	SDRA12	SDRAM_A12	O		SDRAM Interface Address12
		GPIOA26	BI		GPIOA Port 26
38	SDRDQ9	SDRAM_DQ9	BI		SDRAM Interface Data 9
39	SDRDQ10	SDRAM_DQ10	BI		SDRAM Interface Data10
40	SDRDQ11	SDRAM_DQ11	BI		SDRAM Interface Data11
41	SDRDQ12	SDRAM_DQ12	BI		SDRAM Interface Data 12
42	SDRRASB	SDRAM_RASB	O		SDRAM Interface RAS
43	SDRCASB	SDRAM_CASB	O		SDRAM Interface CAS
44	SDRDQ13	SDRAM_DQ13	BI		SDRAM Interface Data13
45	SDRCSB	SDRAM_CSB	O		SDRAM Interface CS
46	SDRGND	SDRAM_GND	PWR		SDRAM Interface GND

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47	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
48	SDRCK	SDRAM_CK	O		SDRAM Interface Clock
49	SDRCKE	SDRAM_CKE	O		SDRAM Interface Clock Enable
50	SDRDQM0	SDRAM_LDQM	O		SDRAM Interface LDQM (for 16bits SDRAM)
51	SDRDQ14	SDRAM_DQ14	BI		SDRAM Data14
52	SDRDQM1	SDRAM_DQM/UDQM	O		SDRAM Interface DQM (for 8bits SDRAM) SDRAM Interface UDQM (for 16bits SDRAM)
53	SDRDQ15	SDRAM_DQ15	BI		SDRAM Interface Data15
54	VBUS	VBUS	I		VBUS
55	UVCC	UVCC	PWR		UVCC
56	DP	DP	BI		Data Plus
57	DM	DM	BI		Data Minus
58	UGND	UGND	PWR		UGND
59	RREF	RREF	AO		Reference Resistance
60	AGNDP	AGNDP	PWR		AGND
61	AVDDP	AVDDP	PWR		AVDD
62	UGNDS	UGNDS	PWR		UGND
63	UVCCS	UVCCS	PWR		UVCC
64	MICINL	MICINL	AI		Microphone In Left Channel
65	VMIC	VMIC	AI		Microphone Power Supply
66	FMINR	FMINR	AI		FM In Right Channel
67	FMINL	FMINL	AI		FM in Left Channel
68	AGND	AGND	PWR		Audio Analog GND
69	AVCC	AVCC	PWRO		Audio Analog VCC
70	VRDA	VRDA	AO		Audio DAC Voltage Reference
71	VREFI	VREFI	AI		Voltage Reference Input
72	PAGND	PAGND	PWR		Audio PA GND

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73	AOUTR	AOUTR	AO		Audio output Right Channel
74	PAVCC	PAVCC	PWRO		Audio PA VCC
75	AOUTL	AOUTL	AO		Audio output Left Channel
76	AVDD	AVDD	PWRO		Audio VDD
77	HOSCO	HOSCO	AO		High Oscillator Output
78	HOSCI	HOSCI	AI		High Oscillator Input
79	VCC	VCC	PWRI		VCC
80	KSIN2	KSIN[2]	BI	1	Key Scan Input2
		GPIOA10	BI		GPIOA Port 10
81	KSOUT2	KS_OUT[2]	BI	1	Key Scan output 2
		GPIOB22	BI		GPIOB Port 22
82	KSIN1	KS_IN[1]	BI	1	Key Scan Input 1
		GPIOA9	BI		GPIOA Port 9
83	KSOUT1	KS_OUT[1]	BI	z	Key Scan Output 1
		GPIOA13	BI		GPIOA Port 13
84	KSIN0	KS_IN[0]	BI	1	KEY Scan in 0
		GPIOA8	BI		GPIOA Port 8
85	KSOUT0	KS_OUT[0]	BI	z	Key Scan Output 0
		GPIOA12	BI		GPIOA Port12
86	CEB3	NF_CEB3	O		NAND FLASH Interface CE3
87	RESETB	RESETB	I		System RESET
88	TEST /CLKOUT	TEST	I		TEST FM Module Clock out
89	I2C1SDA	I2C1_SDA /UART2IR_RX	BI	z	I2C1 Interface SDA UART2 or IrDA Interface RX
		GPIOA7	BI		GPIOA Port 7
90	I2C1SCL	I2C1_SCL /UART2IR_TX	BI	z	I2C1 Interface SCL UART2 or IrDA Interface TX
		GPIOA6	BI		GPIOA Port 6
91	BL_NDR	BL_NDR	AO		Back Light NDR

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92	REM_CON	REM_CON	AI		Remote Control ADC input
93	BL_FB	BL_FB	O		Back Light Feed Back
94	IO_VDD	IO_VDD	PWR		POWER Pin IOVDD
95	LXVDD	LXVDD	PWR		POWER Pin LXVDD
96	PGND	PGND	PWR		POWER MOS GND
97	PGND	PGND	PWR		POWER MOS GND
98	LXVCC	LXVCC	PWR		POWER Pin LXVCC
99	IO_VCC	IO_VCC	PWR		POWER Pin IOVCC
100	BAT	BAT	PWRI		Battery input
101	DC5V	DC5V	PWRI		DC5V input
102	VCC	VCC	PWRIO		VCC
103	VDD	VDD	PWRIO		VDD
104	VCCOUT	VCCOUT	PWRO		Programmed VCC output
105	GND	GND	PWR		GND
106	CEB6	SD_CLK /CE6	O	1	SD CARD Interface CLOCK LCD Interface CE6
		GPIOB29	BI		GPIOB Port 29
107	A0	NF_ALE /RGB_WD[0]	O	0	NAND FLASH ALE RGB Interface Data0
		GPIOA0	BI		GPIOA Port 0
108	A1	NF_RB /RGB_WD[9]	O	0	NAND FLASH Interface Ready/Busy RGB Interface Data 9
		GPIOA1	BI		GPIOA Port 1
109	A2	NF_CLE /RGB_RS /SD_CMD	O	0	NAND FLASH Interface CLE RGB Interface RS SD card Interface CMD
		GPIOA2	BI		GPIOA Port 2
110	D0	NF_D[8] /RGB_WD[1] /SD_DAT[0]	BI		NAND FLASH Data 8 RGB Interface Data 1 SD Card Interface Data 0

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111	D1	NF_D[9] /RGB_WD[2] /SD_DAT[1]	BI		NAND FLASH Interface Data 9 RGB Interface Data 2 SD Card Interface Data 1
112	D2	NF_D[10] /RGB_WD[3] /SD_DAT[2]	BI		NAND FLASH Interface Data 10 RGB Interface Data 3 SD Card Interface Data 2
113	D3	NF_D[11] /RGB_WD[4] /SD_DAT[3]	BI		NAND FLASH Interface Data 11 RGB Interface Data 4 SD Card Interface Data 3
114	D4	NF_D[12] /RGB_WD[5] /SD_DAT[4]	BI		NAND FLASH Interface Data 12 RGB Interface Data 5 SD Card Interface Data 4
115	D5	NF_D[13] /RGB_WD[6] /SD_DAT[5]	BI		NAND FLASH Interface Data 13 RGB Interface Data 6 SD card Interface Data 5
116	D6	NF_D[14] /RGB_WD[7] /SD_DAT[6]	BI		NAND FLASH Interface Data 14 RGB Interface Data 7 SD card Interface Data 6
117	D7	NF_D[15] /RGB_WD[8] /SD_DAT[7]	BI		NAND FLASH Interface Data 15 RGB Interface Data 8 SD card Interface Data 7
118	CEB0	NF_CEB0	O		NAND FLASH Interface CE0
		GPIOA16	BI		GPIOA Port 16
119	VDD	VDD	PWRI		VDD
120	D8	NF_D[0] /RGB_WD[10]	BI		NAND FLASH Data 0 RGB Interface Data 10
121	D9	NF_D[1] /RGB_WD[11]	BI		NAND FLASH Interface Data 1 RGB Interface Data 11
122	D10	NF_D[2] /RGB_WD[12]	BI		NAND FLASH Interface Data 2 RGB Interface Data 12

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123	D11	NF_D[3] /RGB_WD[13]	BI		NAND FLASH Interface 3 RGB Interface Data 13
124	D12	NF_D[4] /RGB_WD[14]	BI		NAND FLASH Data 4 RGB Interface Data 14
125	D13	NF_D[5] /RGB_WD[15]	BI		NAND FLASH Interface Data 5 RGB Interface WD 15
126	D14	NF_D[6] /RGB_WD[16]	BI		NAND FLASH Data 6 RGB Interface Data 16
127	D15	NF_D[7] /RGB_WD[17]	BI		NAND FLASH Interface Data 7 RGB Interface Data 17
128	GND	GND	PWR		GND

NOTE:

1 PWR—Power Supply
2 AI—Analog Input
3 AO—Analog Output
4 O—Output
5 I—Input
6 BI—Bi-direction
7 USCU, USCL—Schmitt Type
8 OD—Open Drain
9 ABI—Analog Bi-direction

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3 Function Description

3.1 Functional Block Diagram

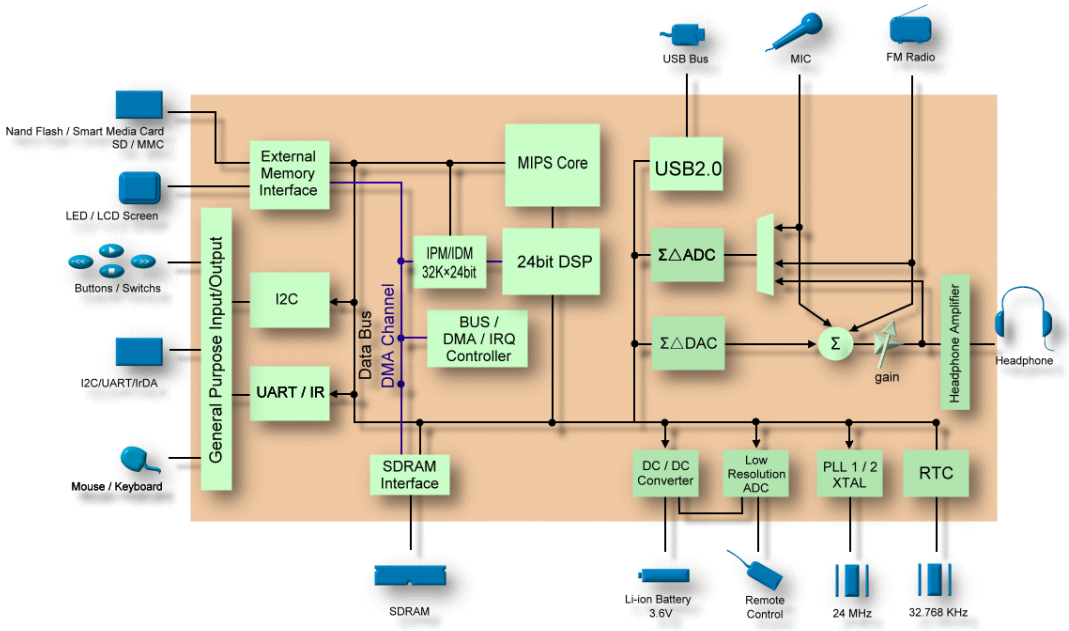

Figure 2: ATJ2135N Functional Block Diagram

3.2 Memory Map

Altogether 4G memory map; user mode 512M: 00000000～1FFFFFFF.

Table 2: ATJ2135N Physical Memory Map

ATJ2135N Physical Memory Map

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Start	End	Size（M）	Function
0x00000000	0x0FFFFFFF	256	SDRAM Space
0x10000000	0x11FFFFFF	32	IO Device
0x12000000	0x13FFFFFF	32	Reserved
0x14000000	0x17FFFFFF	64	IO Device/MEM
0x18000000	0x1FFFFFFF	128	MEM (boot)

IO Map

Start	End	Size（K）	Function
0x10000000	0x1000FFFF	64	PMU/LRADC
0x10010000	0x10017FFF	32	CMU/HOSC
0x10018000	0x1001FFFF	32	RTC/LOSC/WD
0x10020000	0x1002FFFF	64	Interrupt Controller
0x10030000	0x10037FFF	32	SRAM on Chip
0x10038000	0x1003BFFF	16	Reserved
0x1003C000	0x1003FFFF	16	32BitRisc Core Performance CNT
0x10040000	0x1004FFFF	64	Reserved
0x10050000	0x1005FFFF	64	DSP Control
0x10060000	0x1006FFFF	64	DMA Controller
0x10070000	0x1007FFFF	64	SDRAM Controller
0x10080000	0x1008FFFF	64	Reserved
0x10090000	0x1009FFFF	64	Reserved
0x100A0000	0x100AFFFF	64	FLASH I/F
0x100B0000	0x100BFFFF	64	SD IF
0x100C0000	0x100CFFFF	64	MHA
0x100D0000	0x100DFFFF	64	Reserved
0x100E0000	0x100EFFFF	64	USB
0x100F0000	0x100FFFFF	64	YVU2RGB
0x10100000	0x1010FFFF	64	DAC＋PA
0x10110000	0x1011FFFF	64	ADC
0x10120000	0x1012FFFF	64	Reserved
0x10130000	0x1013FFFF	64	Reserved
0x10140000	0x1014FFFF	64	Reserved

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0x10150000	0x1015FFFF	64	Reserved
0x10160000	0x1016FFFF	64	Reserved
0x10160000			IR
0x10170000	0x1017FFFF	64	Reserved
0x10180000	0x1018FFFF	64	IIC
0x10190000	0x1019FFFF	64	Reserved
0x101A0000	0x101AFFFF	64	Key Scan
0x101B0000	0x101BFFFF	64	Reserved
0x101C0000	0x101CFFFF	64	GPIO
0x101D0000	0x101DFFFF	64	Reserved
0x101E0000	0x101EFFFF	64	Reserved
0x101F0000	0x101FFFFF	64	Reserved
		2048	SUM
0x10200000	0x11FFFFFF		Reserved
IO/MEM Map			
Start	**End**	**Size（K）**	**Function**
0x14000000	0x1403FFFF	256k	Reserved
0x14040000	0x1405FFFF	128k/96k	DSP mode 24bit Wide (128k) MIPS mode 32bit Wide (96k)
0x140600000	0x17FFFFFF		Reserved
MEM (LCD and LAN) Map			
Start	**End**	**Size（M）**	**Function**
0x18000000	0x18FFFFFF	16M	Reserved
0x19000000	0x19FFFFFF	16M	Reserved
0x1A000000	0x1AFFFFFF	16M	Reserved
0x1B000000	0x1BFFFFFF	16M	Reserved
0x1C000000	0x1CFFFFFF	16M	CE3 (LCD)
0x1D000000	0x1DFFFFFF	16M	CE2
0x1E000000	0x1EFFFFFF	16M	CE1
0x1F000000	0x1FFFFFFF	16M	CE0 (BROM)

3.3 CMU

ATJ2135N supports two oscillator inputs: 24M and 32.768K.

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Clock Management Unit (CMU) can be driven by a 24M high oscillator and a 32.768k low oscillator.

It provides:

- Four main clocks: MIPS core clock, DSP clock, AHB bus clock, APB bus clock;
- A low oscillator and a real time clock (RTC) module with alarm function.

ATJ2135N has a built-in Watch-Dog circuit.

Two 24bit timers are integrated in this IC. Users may select either low or high oscillator as the source.

3.3.1 RTC/LOSC/Watch Dog/Timers

ATJ2135N has a low frequency oscillator, which can choose a built-in source or an external one. Meanwhile the chip also has RTC (Real Time Clock) with an alarm IRQ. The alarm IRQ can wake up the system. For the purpose of protection, a watch dog circuit is also available in the chip.

There are two Timers, namely, Timer0 and Timer1, which can only count down. The clock of the Timer is APB.

3.4 Interrupt Controller

Interrupt controller supports 32 interrupt sources. It can generate five outputs as interrupt requests 0, 1, 2, 3 and 4. Each of these outputs is connected to CPU core; the following table shows the interrupt controller's connections to CPU.

Table 3 Interrupt Controller Connects to CPU

Interrupt Controller Requests	CPU Interface	CPU Interrupt Request
Request 0	SI_INT[0]	IP2
Request 1	SI_INT[1]	IP3
Request 2	SI_INT[2]	IP4
Request 3	SI_INT[3]	IP5
Request 4	SI_INT[4]	IP6

3.4.1 Interrupt Source

Table 4 shows all the interrupt sources. Please refer to the respective peripheral sections for the details on the interrupt sources.

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Table 4: Interrupt Sources

Interrupt Number	Sources	Type
0	Reserved	High Level
1	Reserved	High Level
2	SD/MMC	High Level
3	MHA	High Level
4	USB	High Level
5	DSP	High Level
6	Reserved	High Level
7	PC (Performance Counter)	High Level
8	2Hz/WatchDog	High Level
9	TIMER1	High Level
10	TIMER0	High Level
11	RTC	High Level
12	DMA	High Level
13	Key	High Level
14	External	High Level
15	Reserved	High Level
16	Reserved	High Level
17	Reserved	High Level
18	IIC1	High Level
19	UART2	High Level
20	Reserved	High Level
21	ADC	High Level
22	DAC	High Level
23	Reserved	High Level
24	NAND	High Level
25	Reserved	High Level
26	YUV2RGB	High Level
27	Reserved	High Level
28	Reserved	High Level
29	Reserved	High Level
30	Reserved	High Level
31	Reserved	High Level

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3.4.2 External Interrupt Sources

Interrupt controller has one external interrupt source, which is input from SIRQ1 and can be configured as level or edge-triggered interrupt. When using external interrupt source, the corresponding multi-function pad must be set as input mode.

3.5 PMU/DC-DC Converter

3.5.1 Description

ATJ2135N PMU includes:

- Two DC/DC Converters, both can work in buck mode. The output voltages can be 3.1V and 1.6V, and programmable.
- Two regulators, whose output voltages are 3.1V and 1.6V, and programmable.
- A bias current generator.
- An oscillator, outputs a signal for DC-DC converters and a 32KHz signal for RTC.
- 6 bits low speed ADC, whose input range is from 0.7V to 1.5V, monitors batteries voltage.
- 4 bits low speed ADC, whose input range is form 0V to 3.1V, monitors remote control signal.
- Battery charger, support Li+ battery.
- VCC voltage detector, VDD voltage detector, Power OK signal (PWROK) generator.
- A PFM - Modulated high voltage DC/DC converters for LED.

PMU Working Mode

- Li+ Battery, 2 Inductors
- Li+ Battery, 1 Inductor for VCC
- Li+ Battery, 1 Inductor for VDD
- Li+ Battery, No Inductor
- External power

3.5.2 DC/DC Converter and Regulator

There are two DC-DC converters and two Regulators in ATJ2135N. Each DC-DC converter can work in buck mode for different input voltage. It also can work in PFM for

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different load current. An ECL PFM converter is built-in.

Table 5: DC/DC Converters & Regulators–Power Mode Set

DC5V>4.3V	DC-DC1	DC-DC2	Regulator1	Regulator2	Description
N (No)	Buck	Buck	N	N	Li+, 2 Inductors
N	Buck	N	N	From BAT	Li+, 1 Inductor for VCC
N	N	Buck	From BAT	N	Li+, 1 Inductor VDD
N	N	N	From BAT	From BAT	Li+, No Inductor
Y(Yes)	N	N	From DC5V	From VCC	External power

Table 6: DC/DC Converters & Regulators—Loading Capacity

Block name	Loading
DC-DC1	3.3V, 200mA @ BAT=4.2V, buck mode
DC-DC2	1.8V, 250mA @ BAT=2.4/3.0V, buck mode
ECL PFM	11—16V, 20—30mA
Regulator1	3.3V, 200mA @ BAT=4.2V
Regulator2	1.8V, 200mA @ BAT=4.2V

3.5.3 Battery Monitor

There is a low speed 6 bits ADC in ATJ2135N for Battery Monitor.

Table 7: Relationship between Battery Type & ADC Input Range

Battery type	Internal Voltage divider for battery	Input range
1 Li+	1/3	1.0-1.4

3.5.4 Remote Control ADC

There is a low speed 4 bits ADC in ATJ2135N for remote control. The input range is from 0 to AVCC.

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3.5.5 Charger Circuits

- Constant current charge
  Default is 200mA; software can set control bit to change it.
- Constant voltage charge 4.2V for Li+ battery.
- Battery voltage
  Li-ion's voltage range is from 2.9V to 4.2V
- Charge Style
  Linear charger for Li+ battery;
  UVLO changes from low go high at 4.3V, high go low at 3.75V.

3.5.6 PWM Back-Light IC Control

In ATJ2137N PMU, a programmable PWM signal generator is integrated for PWM Back Light IC. Its application diagram is as follow.

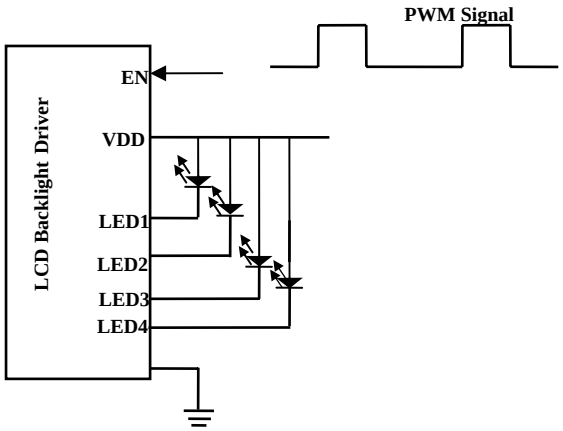

Figure 3: PWM Back Light IC Application Diagram

The built-in block diagram is as follow. There are 8 clock sources of the PWM can be configured. The PWM signal can be programmed up to 32-level duty. All together, PWM signals with 8 frequencies can be outputted. They are 1k, 500, 250, 125, 94k, 47k, 23k and 12k.These frequencies can meet most PWM back light IC application.

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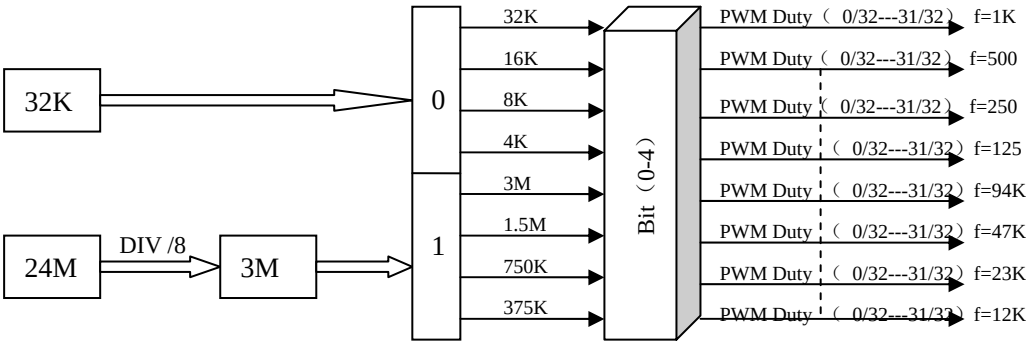

Figure 4: PWM Block Diagram

3.5.7 Signal Description

- DC-DC1 PIN: LX_VCC, IO_VCC.
- DC-DC2 PIN: LX_VDD, IO_VDD.
- High voltage regulator input and output PIN: DC5V, VCC
- Low voltage regulator output PIN: VDD
- Battery input/output PIN: BAT
- DC-DC NMOS ground: PGND
- BL PFM DC/DC PIN: BL_NDR, BL_FB
- Remote control ADC input: REM_CON

3.6 32-BIT RISC Core

The core follows MIPS 4KEc SPEC. This chapter describes the features of RISC Core which are not implemented or different from MIPS 4KEc SPEC.

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3.6.1 Coprocessor 0

In MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics capability, the operating modes (kernel, user and debug) and whether interrupts are enabled or disabled.

3.6.2 Exceptions

The chip implements MIPS 4KEc compliant exception scheme. The scheme consists of the exception vector entry points in both KSEG0 and KSEG1, and the exception code (ExcCode) encodings the nature of the exception. The exception causes include interrupts, debug, execution error conditions, control conditions, and MMU conditions.

The chip implements a MIPS 4KEc compliant interrupt mechanism in which eight interrupt sources are presented to the core. Each interrupt source individually is able to either enable or disable the core from detecting the interrupt. Interrupts are generated by software, integrated interrupt controller, and timer, as noted in Table 9.

Table 8: CPU Interrupt Sources

Interrupt Sources	Interrupt request	Interrupt Mask
Software Interrupt 0	IP0	IM0
Software Interrupt 1	IP1	IM1
Interrupt Controller	IP2~IP6	IM2~IM6
Timer	IP7	IM7

3.6.3 Performance Counters

Performance counters are typically configurable to allow the counting of a variety of processor events. The counters can be read and configured by software. Monitoring software can periodically read the registers or can be configured to signal an interrupt when the counter overflows. A system designer can use performance counters to profile software and hardware performance.

On this chip two performance counters are configurable to count one or two MIPS 4KEc core events, which are fetched from Performance Monitoring (PM) interface or EC bus interface. Therefore the relative frequency of different events can be compared to a large sample set, for example, the ratio of D-cache hits to misses, or the ratio of micro TLB misses

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to instructions completed. Figure 3 shows the performance counters block diagram.

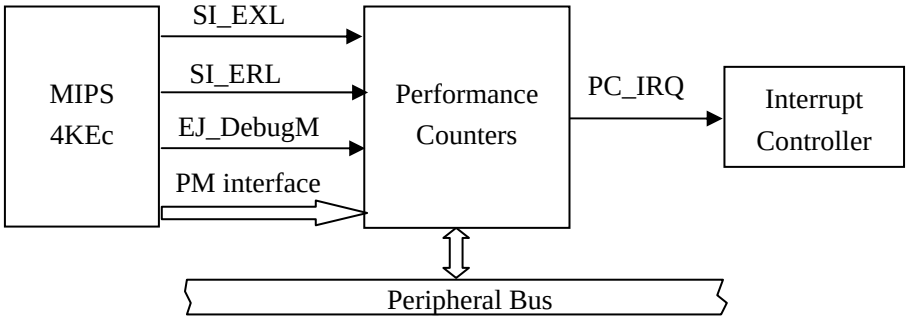

Figure 5: Performance Counters Block Diagram

3.6.4 Other Reference

Please refer to
MIPS32. 4KE. Processor Core Family Software User's MIPS32. 4KE. Processor Core Family Integrator's Guide:MD00104-2B-4KE-ING-02.00.pdf
Manual: MD00103-2B-4KE-SUM-02.02.pdf
MIPS32. 4KEc. Processor Core Datasheet:MD00111-2B-4KEC-DTS-02.00.pdf
MIPS32. Architecture For Programmers Volume I: Introduction to the MIPS32.Architecture:MD00082-2B-MIPS32INT-AFP-02.00.pdf
MIPS32. Architecture For Programmers Volume II: The MIPS32. Instruction Set:MD00086-2B-MIPS32BIS-AFP-02.00.pdf
MIPS32. Architecture For Programmers Volume III: The MIPS32. Privileged Resource Architecture:MD00090-2B-MIPS32PRA-AFP-02.00.pdf
MIPS32. Architecture for Programmers Volume IV-a: The MIPS16e. Application-Specific Extension to the MIPS32.Architecture:MD00076-2B-MIPS1632-AFP-02.00.pdf
MIPS32. Architecture for Programmers Volume IV-d: The SmartMIPS.Application-Specific Extension to the MIPS32.Architecture:MD00101-2B-SMARTMIPS32-AFP-02.00.pdf
Core Coprocessor Interface Specification:MD00068-2B-COPROC-SPC-01.16.pdf

3.7 SDRAM Interface

SDRAM interface can support both SDRAM (Synchronous DRAM) and Mobile SDRAM. It has the following features:

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- Supports SDRAM and Mobile SDRAM
- Separate I/O power supply supporting 1.8V, 2.5V and 3.3V
- Supports 3.3V SDRAM of clock frequency up to PC100
- Supports 3.3V SDRAM of capacity up to 32Mbits
- Supports 3.3V/2.5V/1.8V Mobile SDRAM of Clock frequency up to PC100
- Supports 3.3V/2.5V/1.8V Mobile SDRAM of capacity up to 32Mbits
- Thirteen address signals and one bank address signal
- Access to SDRAM in Byte, Half Word are supported
- Supports up to 23 address bits, 13 for row address, and 10 for column address
- Three clock sources to be chosen for different application
- Priority of transferring through special channel or AHB bus is programmable
- Supports random read or write operation

3.7.1 SDRAM Signals

Table 9: SDRAM Signals

Symbol	Type	Function
CK	O	**Clock output:** CK is clock output. All outputs are sampled on the positive edge of CLK.
CKE	O	**Clock enable output**
CS#	O	**Chip select output**
RAS#,CAS#,WE#	O	**Command outputs**
DM (UDQM) (LDQM)	O	**Output data mask**
BA0	O	**Bank address outputs**
A0~A12	O	**Address outputs**
DQ	I/O	**Data input/ output:** bi-directional data bus.
NC		**No connect:** No internal electrical connection is present.
VDDQ	PWR	**DQ power supply:** **For SDRAM, voltage:** 3.3V +/- 0.3V **For Mobile SDRAM, voltage: 3.3V or 2.5V or 1.8v**
VSSQ	PWR	**DQ ground**
VDD	PWR	**Power supply:** **For SDRAM, voltage:** 3.3V +/- 0.3V **For mobile SDRAM, voltage: 3.3V or 2.5V or 1.8v**
VSS	PWR	**Ground**

Note:

1: **I** for **Input**

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2: **O** for **Output**

3: **PWR** for **Power Supply Signal**

4: Typical logic high voltage of all input or output depends on the value of SV bits in SDRAMPARA register. If SV bits are set to be 1, select 3.3v, and 10 for 2.5v, 01 for 1.8v.

3.8 SRAM on Chip

ATJ2135N has 96k-byte SRAM which can map 24k*32bit (for MIPS) or 32k*24bit (for DSP). It can be operated in byte and possesses BIST test function.

3.9 BROM

Built-in boot ROM in ATJ2135N. MIPS can be selected to boot up from Boot ROM.

3.10 DMA/Bus Arbiter

ATJ2135N DMA controller contains 8 tasks, which are divided into two types, bus DMA and special channel DMA. System bus adopts the subset of AMBA bus protocol.

There are six slaves with double ports, the system bus and DMA special port. They are: SDRAM, DSPMEM, NAND, SD, USB and YUV.

Other slaves are only with system bus, or APB bus. They are: DAC, ADC.

3.10.1 DMA Architecture

DMA controller in ATJ2135N is a special master with four independent special channels to high-speed AHB slaves. Since these six special slaves have two access ports, the slave has to decide which port enjoys higher priority. A register in the slave to set which port enjoys higher priority.

Each DMA task can be set as priority.

DMA0~DMA3 can be transferred through bus only, DMA4~DMA7 can be transferred only through the special channel.

The slave perhaps has two DRQ and DACK.

Some slave devices have address bus, such as SDRAMIF, SRAMOC while others do not have one, such as FLASH port. However, the control register can be accessed through AHB bus, no matter through the special channel access or not.

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3.10.2 DMA Bus Timing

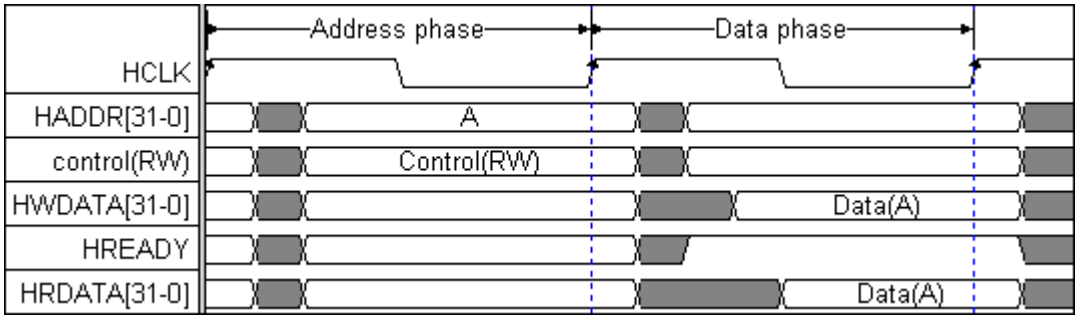

Figure 6: DMA Basic Bus Timing

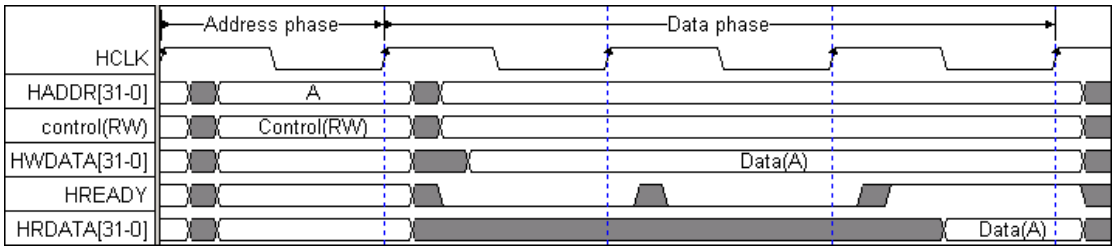

Figure 7: DMA Bus Timing with Wait States

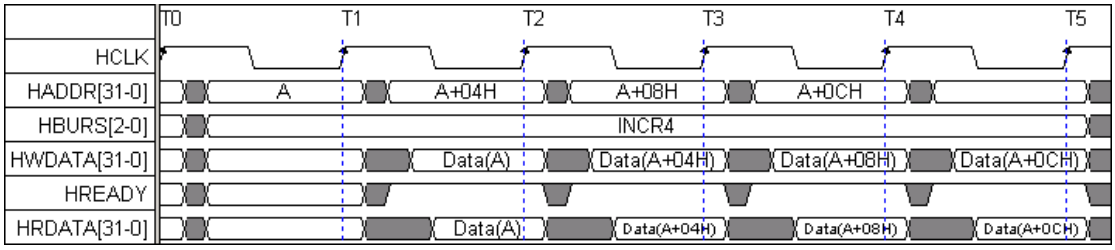

Figure 8: DMA Bus Burst Timing

3.11 24-BIT DSP Core

3.11.1 Features

DSP Core has the following features:

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- Read ADC data directly
- Write some DAC/ADC control register
- With Byte selection function
- 24bit instruction and data bus
- 1 instruction per machine cycle
- Maximum 90 Million Instructions Per Second (MIPS) and extra mass production margin
- One 56bit MAC result register including extension byte
- Parallel 24 x 24 bits multiply-accumulate in 1 instruction cycle
- Fractional and integer arithmetic with rounding mode
- Hardware nested DO loops up to 4 layers
- 16K x 24 bits of Access Program Memory space (IPM)
- 16K x 24 bits of Access Data Memory space (IDM)
- 8bit Parallel Host Interface Port
- Independent Arithmetic/Logic (ALU), Multiplier/Accumulator (MAC) and Barrel Shifter (BASH) Computational Units
- Two Independent Data Address Generators (DAGS)
- Automatic Booting of Internal Program Memory through Host Interface Port (HIP)
- Stand-alone ROM Execution (Optional)
- Built-in Debug Support Unit (DSU)
- Full static design for operating frequencies up to 96MIPS or down to 0 Hz
- On-chip Harvard architecture permitting simultaneous accessed to PM and DM

3.12 Media Hardware Accelerator (MHA)

3.12.1 Description

MHA (Media Hardware Accelerator) is a coprocessor for image or video processing. It supports the following processing: DCT (Discrete Cosine Transform), IDCT (Inverse DCT), Q (Quantization), IQ (Inverse Q), IDRO (Input Data Reorder), ODRO (Output Data Reorder), LS (Level Shift) and ILS (Inverse Level Shift). Table 10 shows all the processing and their applications.

Table 10: Functions and Application of MHA

Applications / Processing	JPEG/Move JPEG Encoder	JPEG/Move JPEG Decoder	MPEG1,MPEG2,MPEG4	MPEG1,MPEG2,MPEG4	H2.63 / H2.63+ Encoder	H.263/ H2.63+ Decoder

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			Encoder	Decoder		
DCT	Y	-	Y	-	Y	-
IDCT	-	Y	S	Y	S	Y
JPEG Q	S	-	-	-	-	-
JPEG IQ	-	S	-	-	-	-
H.263 Q	-	-	S	S	S	-
H.263 IQ	-	-	S	S	S	S
MPEG IQ	-	-	S	S	-	-
IDRO	-	S	S	S	S	S
ODRO	S	-	S	S	S	S
LS	S	-	S	S	S	S
ILS	-	S	S	S	S	S
CLIP	-	-	S	S	S	S

Note: Y is necessary processing; S is optional processing; - is unused processing.

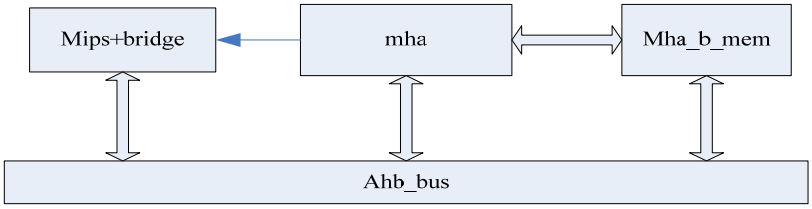

Figure 9: How to Use MHA in a System

3.12.2 Features

- When MHA is busy, RISC can access to the other blocks.
- MHA data buffer can be accessed with DMA, without the special channel.
- MHA can be controlled by MCU with IO registers, and its status can read by MCU at any time.
- MHA will send interrupt signal to MCU when one or more blocks accomplish the processing. The block number can be set as a maximum of 8.
- MHA supports 8bit per sample mode and 9bit per sample mode processing. For 8bit mode, the valid width of DCT input data is 8bit and output data is 11bit, the valid width of IDCT input data is 11bit and output data is 8bit. For 9bit mode, the valid width of DCT input data is 9bit and output data is 12bit, the valid width of IDCT

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input data is 12bit and output is 9bit.

- MHA has two modes for input data and output data: normal order mode and "Z" scanning mode.
- MHA can enable or disable level shift or inverse level shift processing.
- MHA supports optional Q and IQ processing: JPEG Q and IQ, H.263 IQ, MPEG4 IQ. In every Q or IQ processing, it can be chosen from one of 4 Q tables, which is stored in normal order mode.
- Division is replaced by multiplication to reduce the hardware area; since its result equals the dividend multiply the divisor's reciprocal.
- There are two 512x16bits buffer blocks within the MHA. They are used in turn by IO registers. When one block is used for data processing, the other one can be used for data transfers.
- The MHA can accomplish one block processing within 3us, which can satisfy the MJPEG (4:2:0) encoding or decoding with 640x480 30fps or 720x576 25fp.
- MHA data bus is 32bit width, which contains two data of 16bit. The following table shows the data bus.

31 16	15 0
Data1	Data0

Figure 10: MHA data bus

- MHA can auto write zero to memory after read, with which can lessen time of software write zero.
- MHA can close and open the clip function which clips the output data to 0 ~255 after IDCT of 9bits mode. Clip always be applied in decoder for intra frame.
-

3.13 NAND FLASH Interface

The general purpose Nand Flash Interface controller is a State Machine configurable interface to external Nand Flash/SMC. The highly configurable and flexible interface can attach to using most of readily available Nand Flash device. The flash data bus can be configured to be 8bit or 16bit access.

The flash State machine provides automatic timing control for the using data read and write access signal line. The interface automatically maintains proper CLE,ALE and CE setup and hold up as well as proper read/write DMA practical. The Controller will transfer the data between the Int_RAM Mem and ext_Flash Mem by AHB or DMA.

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The Controller module can monitor the relatively interval transitions of the NAND flash device's Ready/Busy signal. This include an interrupt that can monitor the rising edge of the busy signal and that can be set generate a timeout interrupt if the NAND flash device hang up, etc.

The forward error correction module is used to provide ATJ2137N applications with a reliable interface to various storage media, especially storage media that would otherwise have unacceptable bit error rates. The ECC module comprises two different error correcting code processors:

- 1-bit correcting Hamming-code encoder/decoder.
- 8-bit correcting BCH encoder/decoder

The 1-bit hamming code is defined by Samsung for use with compliant NAND flash memories. This code is capable of correcting a single incorrect bit over the block for which the ECC is valid (256 bytes).

The purpose of the BCH decoder is to process a coded block (data block followed by "parity" check data) to determine if there is an error and, if there are errors, where they are located and how to correct them. The purpose of the BCH encoder is to read a block of 512-symbols from RAM, calculate and append 13-parity symbols to form a 516-symbol BCH-codeword.

The Hamming code error corrector is strong enough to detect two bits in error in 256bytes and to correct 1-bit/256 byte errors. Both of these error correction encoder/decoders use DMA transfers to move data to and from on-chip RAM completely in parallel with the MIPS performing other useful work.

Six byte address support for new NAND Flash support
SLC & MLC NAND Flash support
16 bit wide NAND support
50nm NAND flash support
Monitor the NAND flash Ready/Busy signal support

3.14 SD/MMC Interface

SD/MMC Interface is based on MMC card SPEC 4.1 and is compatible with SD memory card physical layer SPEC version 1.01. Multimedia Card/SD is a serial input/output interface to send command and receive data. Its features are as follows:

1. Supports SD memory card, MMC memory card.
2. Supports 1bit, 4bit, 8bit, bus mode.
3. Clock max rate up to 52MHz.
4. Data transfer FIFO and DMA control.
5. Read /Write CRC Status Hardware checked automatically.

3.15 YUV2RGB Interface

The module performs the image data transfer from frame buffer to LCD panel. It accelerates the frame data displayed by hardware operation. It is optional and mainly used

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in movie decoding. The processes include:

1. Up-sampling from YUV 422 to YUV 444
2. Change from YUV / YCbCr to RGB (8,8,8) format

YCbCr to RGB:

R = Y + 1.402 *(Cr-128)

G = Y - 0.34414*(Cb-128) - 0.71414*(Cr-128)

B = Y + 1.772 *(Cb-128)

YUV to RGB:

R = Y + 1.14V

G = Y - 0.39U - 0.58V

B = Y + 2.03U

3. Cut down RGB (8, 8, 8) to the RGB format required in LCD Panel.

3.16 USB2.0 SIE

3.16.1 General Description

ATJ2135N USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

3.16.2 Features

- Fully compliant with USB Specification 2.0.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports Session Request Protocol (SRP).
- Supports full-speed or high-speed in peripheral mode.
- Supports 4 IN endpoint and 4 OUT endpoint except endpoint0.
- Supports high-speed high-bandwidth Isochronous and Interrupt transfer.
- Configurable endpoint buffer size, direction and endpoint transfer type.
- Integrated asynchronous RAM as endpoint buffer.
- Supports Bulk transfer.
- Supports suspend, resume and power managements function.

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- Supports remote wakeup.

3.17 I2C Interface

ATJ2135N has I2C Interface, which can be configured as either master or slave device. In master mode, it generates the clock (I2C_SCL) and initiates the transactions on the data line (I2C_SDA). The data on the I2C bus is byte-oriented. Multi-Master mode, 10-bit address and hi-speed mode are not supported. See the **I2C_Bus_Specification_1995** for the details.

Pull-up resistor is necessary on the I2C line as all of the I2C drivers are open drain. External 2k-Ohm resisters are typically used to pull the signals up to VCC.

3.18 UART Interface

ATJ2135N contains UART interface and it has the following features:

- 5-8 Data Bits and LSB first in transmitting and receiving.
- 1-2 stop bits
- Even, Odd, Logic0, Logic1, Parity and No Parity are supported.
- 8-byte transmit and receive FIFO
- Interrupts for receiving FIFO half full and not empty
- Interrupts for transmit FIFO empty and half empty
- Capable of speeding up to 1.5Mbs to enable the connections with Bluetooth and other peripherals.
- Has Infrared Data Association (IrDA) inputs and outputs (Optional)

3.19 IR Interface

IrDA is a standard defined by IrDA consortium (Infrared Data Association). It specifies the way to transfer data via infrared radiation wireless. The IrDA specifications include standards for both the physical devices and the protocols used to communicate with each other. IrDA devices conform to standards IrDA 1.0 and 1.1.

Speed for IrDA v1.0 ranges from 2400bps to 115200bps. Pulse modulation with 3/16 of the length of the original duration of a bit is used. Data format is the same as a serial port asynchronously transmitted word, with a start bit at the beginning.

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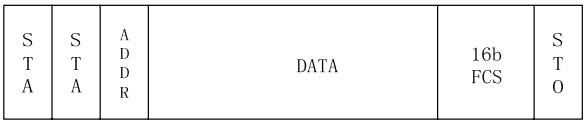
IrDA v1.1 defines the speed 0.576 and 1.152 Mbps for MIR mode and 4Mbps for FIR mode with 1/4 mark-to-space ratio.

For MIR mode, the basic unit (packet) is transmitted synchronously, with a starting sequence at the beginning. A packet consists of two start words followed by a target address (IrDA devices are assigned numbers by the means of IrDA protocol, so they are able to unambiguously identify themselves), data, CRC-16 and a stop word.



STA: Beginning Flag, 01111110 binary
ADDR: 8 bit Address Field
DATA: 8 bit Control Field plus up to 2045=(2048-3) bytes information Field
FCS: CCITT 16 bit CRC
STO: Ending Flag, 01111110 binary

Figure 11: Packet for MIR Mode

For FIR mode, two bits are encoded in a pulse within one of the four possible positions in time. Therefore the information is carried by the pulse position, instead of pulse existence as in previous modulations. With the bit speed of 4Mbps, the transmitter flashes at 2MHZ rate. However, unlike 0.576 and 1.152 Mbps, 4Mbps packets use CRC-32 correction code.

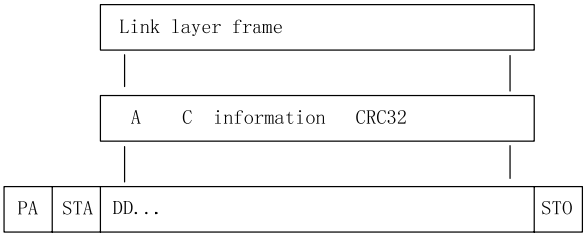


Figure 12: Packet for FIR Mode

ATJ2135N supports SIR, MIR and FIR mode and has 16bit and 32bit hardware CRC generation and detection.

The simultaneous application of UART2 and IR is not allowed since they have some common register.

UART/IR BaudRate (baud rate) must be selected by setting the UART2_CLK_CTL Register of the CMU.

Supports IrDA mode.

Table 11: IR Interface Modes

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Mode	Speed	CLK setting	Compliance
SIR	2.4 to 115.2kbps	Depend on the UART2_CTL bit 23: When select pulse width 3/16 bit : BaudRate*16=CORE_CLK/UART2_CLK_DIV When select pulse width 1.6u, (support baudrate from 9600 to 115200 bps) BaudRate*16*16= CORE_CLK/UART2_CLK_DIV	IrDA 1.0
MIR	0.576 and 1.152 Mbps	BaudRate*8=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection
FIR	4 Mbps	24M=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection

3.20 Key Scan

The Key Scan supports parallel mode and serial mode. The max scan matrix in serial mode is 3x16. There are 4 key scan data registers. For each byte (there are 4 bytes for each register), only the low 3 bits are valid.

In parallel mode, the max scan matrix is 3x3 and is shown as follows:

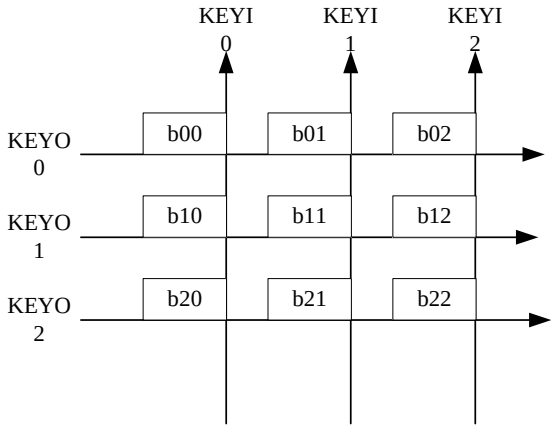

Figure 13: Max Key Scan Matrix in Parallel Mode

In the serial mode, one or more external shift register chips should be used. The following is an 3x8 scan matrix example.

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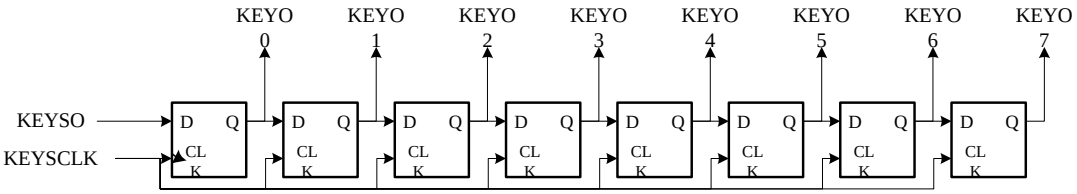

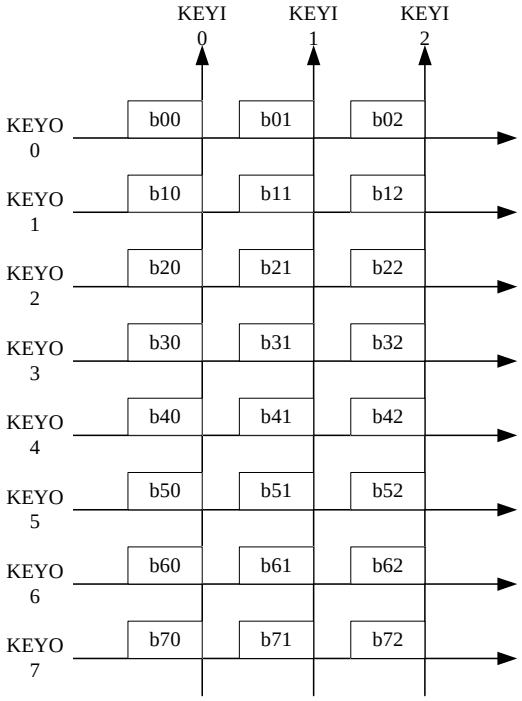

Figure 14: 3*8 Key Scan Matrix in Serial Mode

Note: KEYSO is PIN KEYO1, KEYSCLK is PIN KEYO0.

The whole timing is as follows (parallel mode):

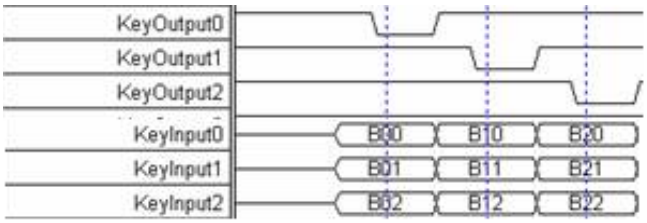

Figure 15: The Whole Key Scan Timing

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In serial mode, two external 8bit shift registers can be used at last, that is to say, the maximum scan matrix is 3x16.

3.21 DAC and Headphone Driver

ATJ2135N's internal DAC is an on-chip Sigma-Delta Modulator of which a high performance DAC is composed. DAC interface supports 8-level playback FIFO (16 X 24bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz).

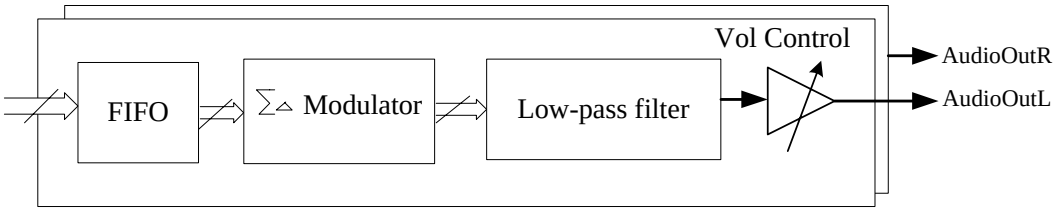

Figure 16: DAC Block Diagram

3.22 ADC

Internal microphone amplifier has gain for recording. VMIC pin is the power supply (2.57V) for microphone.

Audio ADC is a 21bit Sigma-delta Analog-to-digital Converter. Its input source can be selected from MIC amplifier or external FM, and it has two FIFO.

Fs supports 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.

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4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	1.5	2.1	V
	VCC	2.8	3.4	V
Input voltage	V_{IH}	2.8	3.4	V
	VIL	2.8	0.3	V
Junction Temperature	T_j		150	℃
Lead Temperature	(Soldering, 10 sec)		260	℃
Storage temperature	T_{stg}	-65	150	℃

Note:

1. TO = 25℃（Operating Temperature）, VDD = 1.8 V, VCC = 3.1 V
2. Do not short-circuit two or more output pins simultaneously.
3. Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in the DC and AC characteristics are the ranges for normal operation and the quality assurance of the product.

4.2 Capacitance

Table 13: Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		20	pF

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I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		20	pF

Note: T_O = 25℃, VCC = 0 V.

4.3 DC Characteristics

Table 14: DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.9VCC		VCC+0.3	V
Low-level input voltage	V_{IL}		-0.3		0.1VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			±10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			±5	uA

Notes:

1. TA = 0 to +70℃, VDD = 1.8 V, VCC = 3.1 V
2. IVDD is a total power supply current for the 2.5 V power supply. IVDD is applied to the LOGIC and PLL and OSC block.
3. IVCC is a total power supply current for the 3.0 V power supply. IVCC is applied to the USB, IO, TP, and AD block.

4.4 PMU

DC/DC Operating Voltages: When Li-ion mode: DC/DC operates with battery as low as 2.8V.

Table 15: System Standby Dissipation

Parameter	MIN (uA)	Typical (uA)	MAX (uA)
IVCC+IAVCC		100	110
IVDD		40	55
IAVDD		3.5	4.5
RTCVDD		1.0[1]	
		0.3[2]	

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IUVCC		150	175

Note1: When ex osc is enabled.

Note2: When ex osc is disabled.

Table 16: Vccout Load Capability

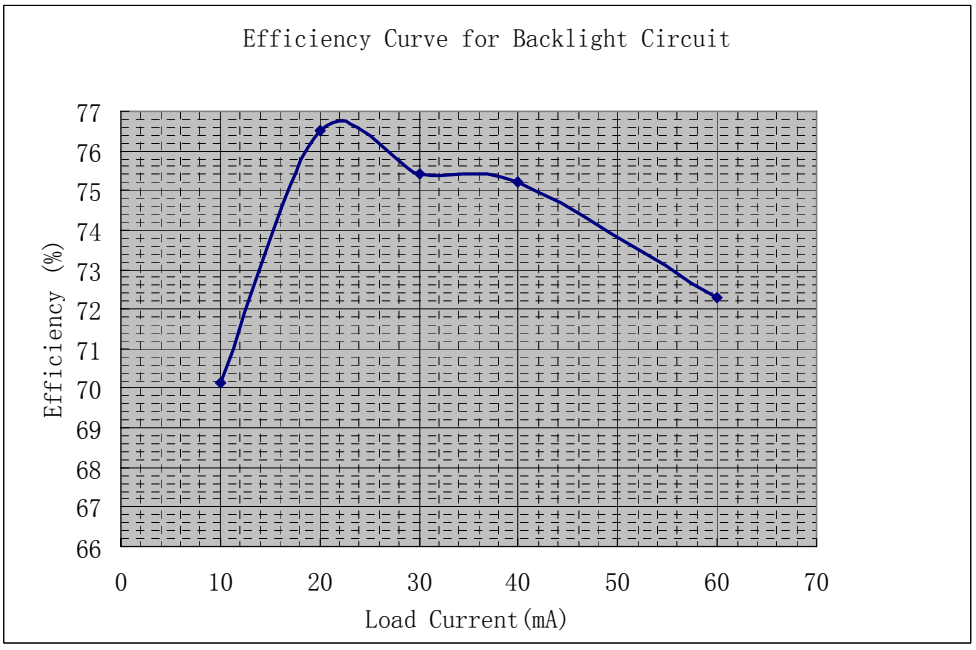
Parameter	MIN (mA)	Typical (mA)	MAX (mA)
IVCCOUT	22	25	

Note: the parameter is tested when VCC is 3.1V and VCCOUT is 95%VCC.

Table 17: LRADC Precision

ERROR / Parameter	MIN	TYPICAL	MAX	Unit
REMO_ADC	-	-	20	mV
BAT_ADC Li-ION	-	-	50	mV

Figure 17: Efficiency Curve for Backlight Step Up Circuit



It is the ordinary TDK47uH inductor that has been applied in backlight circuit, and the diode is RB491D Schottky.

When Vin=3.6V, Vout=12V

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Figure 18: DC/DC Efficiency Curve 1

(Please refer to the corresponding schematic diagram of reference circuit for DC/DC circuit components)

Li-ION mode: VBAT=3.6V

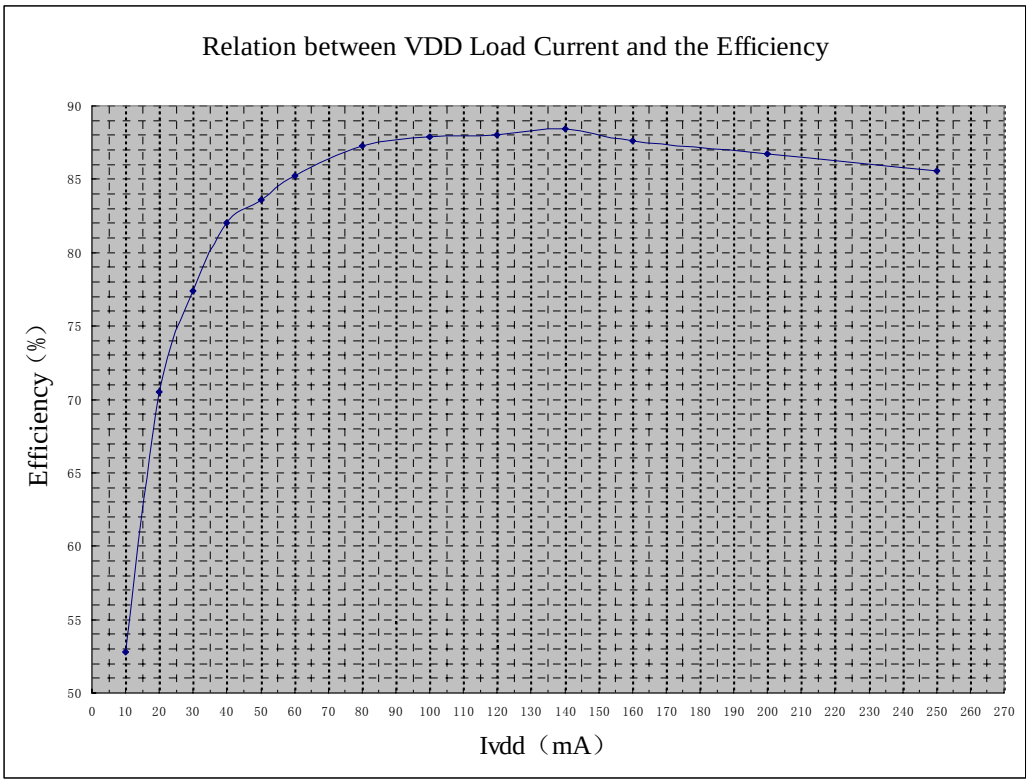

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Figure 19: DC/DC Efficiency Curve 2

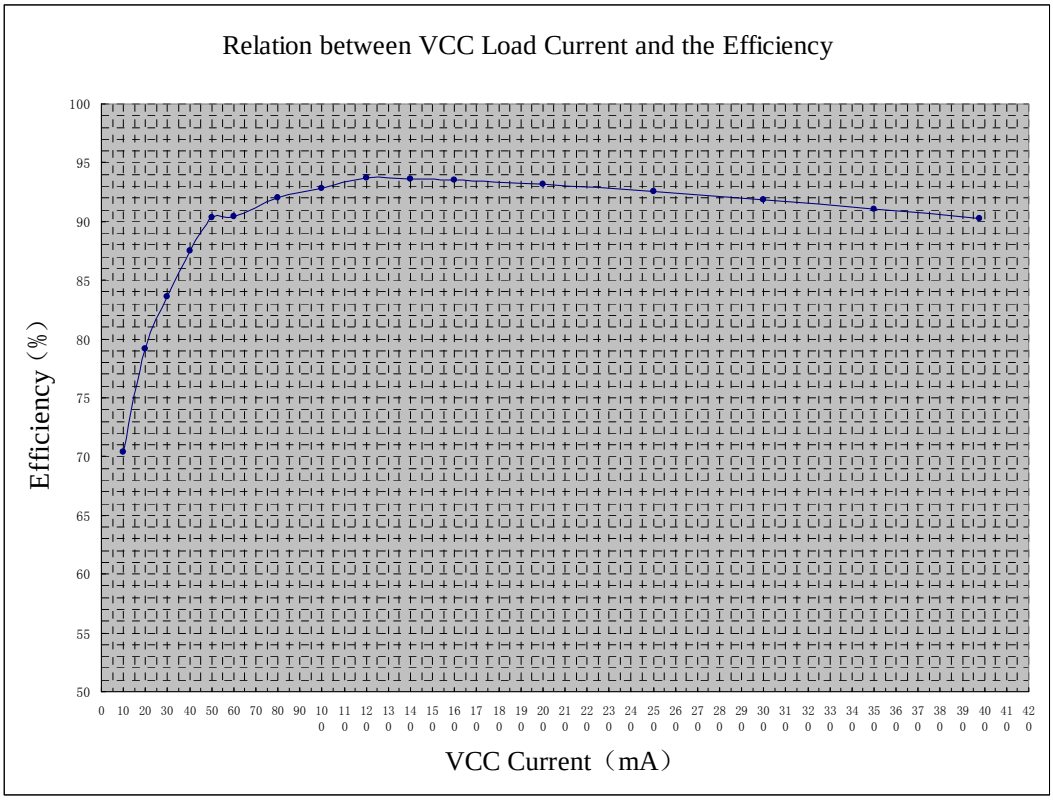

Figure 20: Charging Curve—Voltage Characteristics Curve

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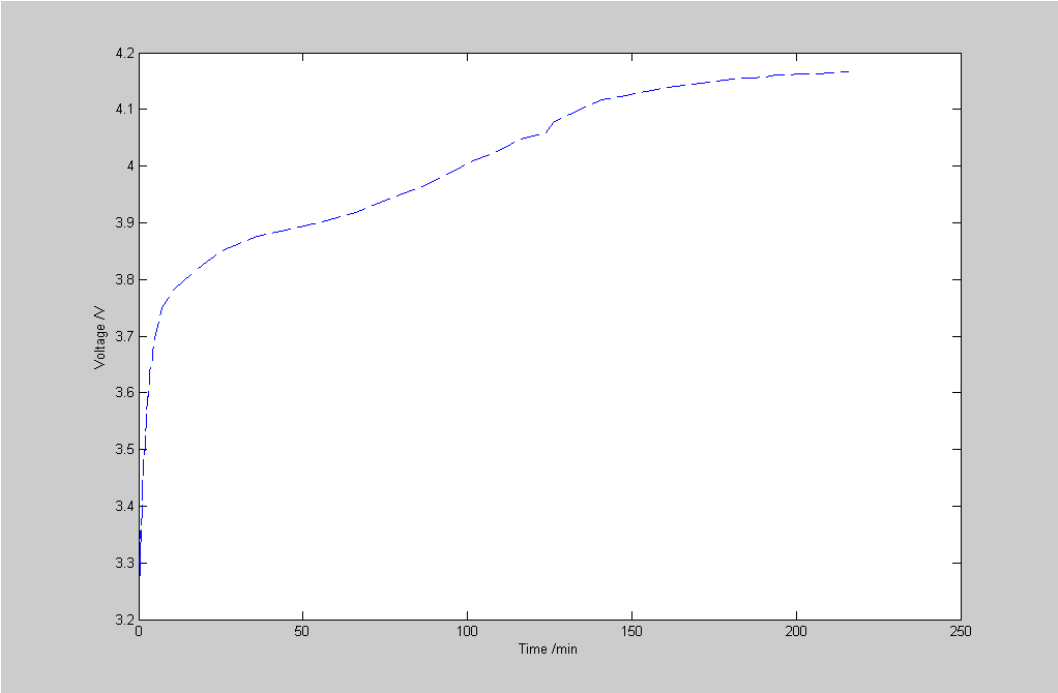
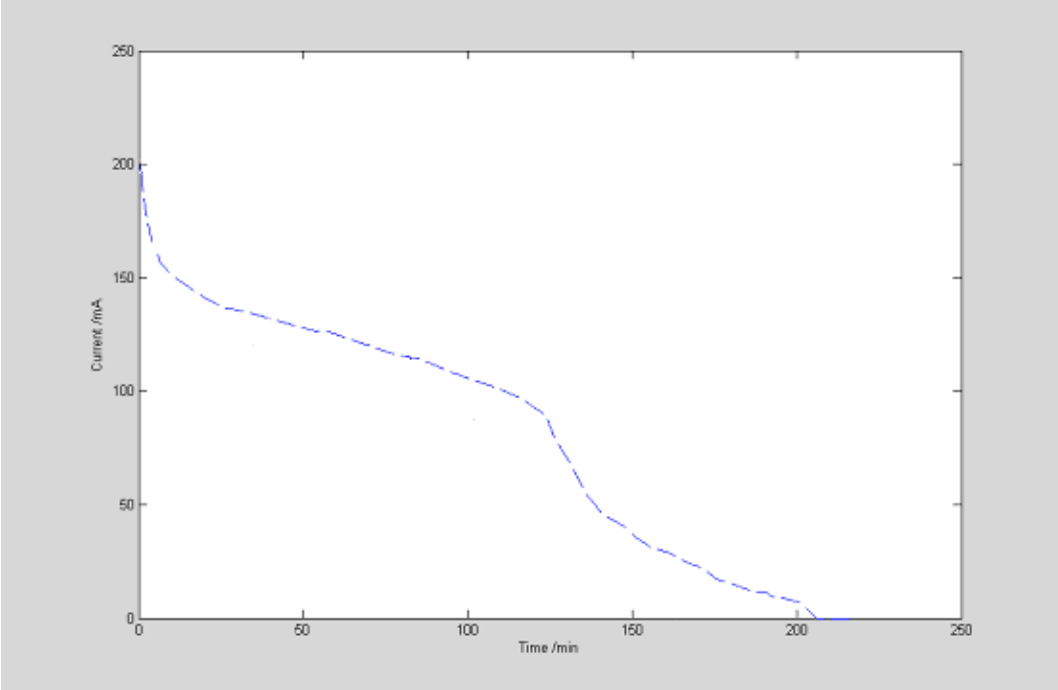


Figure 21: Charging Curve—Current Characteristics Curve



Note: the above results is measured when charging 270mAh Li-ion battery at the charging current of 200mA.

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Table 18: LDO Load Capacity

LDO Input	IVCC			IVDD		
	MIN (mA)	Typical (mA)	MAX (mA)	MIN (mA)	Typical (mA)	MAX (mA)
2.5V				220	240	
3.1V				350	400	
3.6V	320	350		350	400	
4.5V	350	380				
5.0V	420	480				

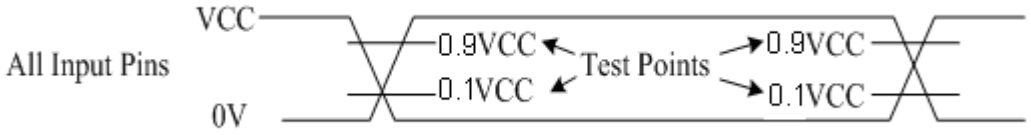
Note: the parameter is tested when VOUT is 95%VIN.

4.5 AC Characteristics

(To = 0 to +70℃, VDD = 2 to 3 V, VCC = 2.7 to 3.6 V)

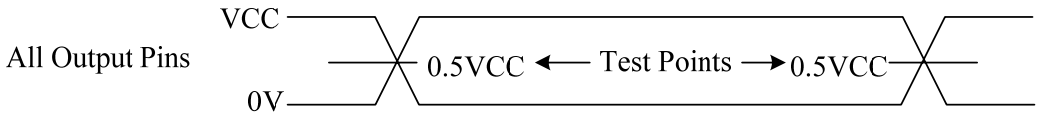
4.5.1 AC Test Input Waveform

Figure 22: AC Test Input Waveform



4.5.2 AC Test Output Measuring Points

Figure 23: AC Test Output Measuring Points



4.6 Reset Parameter

Table 19: Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit

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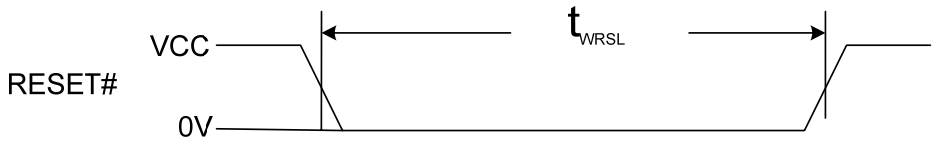
Reset input low-level width	t_{WRSL}	RESET# pin	230		us

Figure 24: Reset Timing

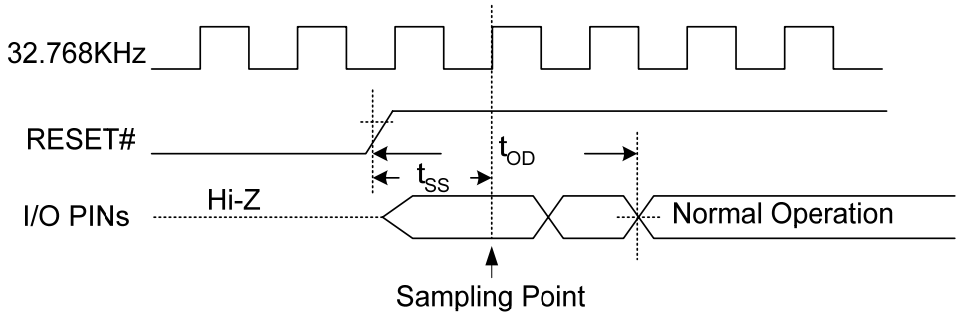


4.7 Initialization Parameter

Table 20: Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}			120	us
Output delay time (from RESET#)	t_{OD}			120	us

Figure 25: Initialization Timing



4.8 GPIO Interface Parameter

Table 21: GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	TYPE	MAX.	Unit
GPIO output rise time	t_{GPRISE}		3		40	ns
GPIO output fall time	t_{GPFALL}		3		40	ns

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Figure 26: GPIO Interface – Output time

Table 22: GPIO Drive

GPIOX（PIN NO/NAME）	Rh (Ω)	IoH（mA）	RL(Ω)	IoL（mA）	Power on status (CEOS=1)
GPIOA17 (4/CEB2)	/	14	/	14	H
GPIOB31 (6/SIRQ1)	/	2	/	2	H—>Z
GPIOA25 (33/SDRA11)	80k	11	70k	11	H—>L
GPIOA26 (37/SDRA12)	80k	11	70k	11	H—>L
GPIOA10 (80/KSIN2)	/	2	/	2	H
GPIOB22 (81/ KSOUT2)	/	2	/	2	H
GPIOA9 (82/ KSIN1)	/	2	/	2	H
GPIOA13 (83/ KSOUT1)	/	2	/	2	Z
GPIOA8 (84/ KSIN0)	/	2	/	2	H
GPIOA12 (85/KSOUT0)	/	2	/	2	Z
GPIOA7 (89/ UART1CTSB)	/	11	/	11	Z
GPIOA6 (90/UART1RTSB)	/	11	/	11	Z
GPIOB29 (106/CEB6)	/	20	/	18	H
GPIOA0 (107/A0)	/	11	/	11	NAND（ALE）—>L
GPIOA1 (108/A1)	/	11	/	11	NAND（RB） —>L
GPIOA2 (109/A2)	/	11	/	11	NAND（CLE）—>H
GPIOA16 (118/ CEB0)	/	11	/	11	H

Notes:

1. Rh is internal pull up resistance, and IoH is drive ability of output H;
2. RL is internal pull down resistance, and IoL is drive ability of output L;
3. Power up status means the status start from BROM;
4. For those GPIO reused with SDRAM (A18-A26), there is HOLD circuit. Its pull up/down resistance status is decided by the previous pad level status in Input Enable status. HOLD circuit is meaningless in output status.

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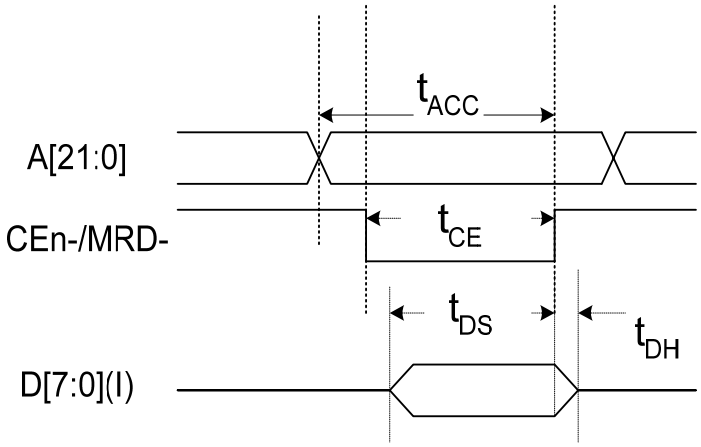
4.9 Ordinary ROM Parameter

Table 23: Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	102		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	82		ns
Data input setup time	t_{DS}	HOSC=24MHz	0		ns
Data input hold time	t_{DH}	HOSC=24MHz	0		ns

Figure 27: Ordinary ROM Parameter



4.10 External System Bus Parameter

Figure 28: External System Bus Timing

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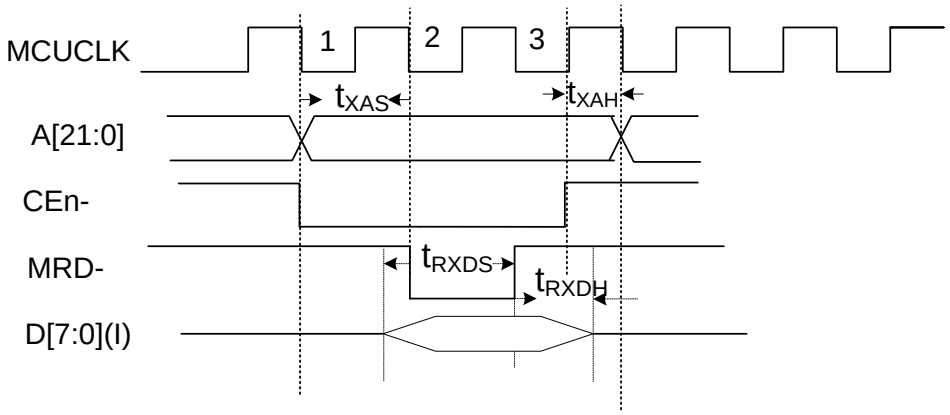

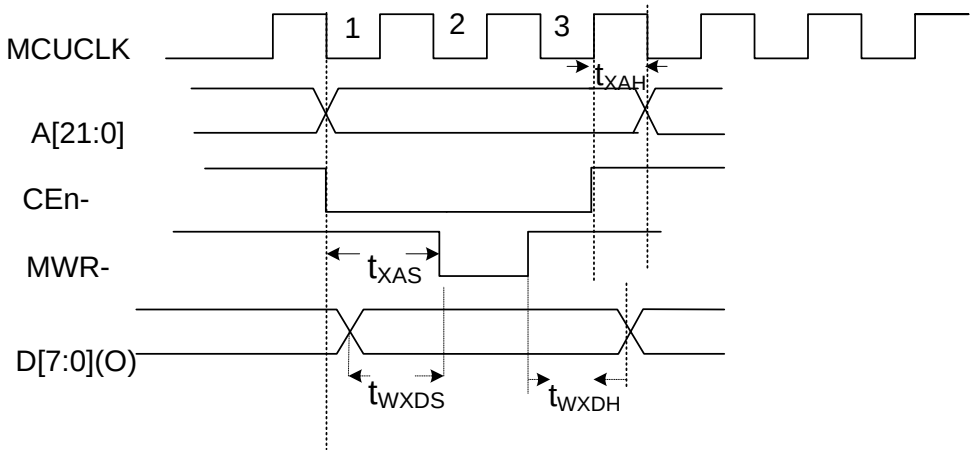

Table 24: External System Bus Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	25		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns

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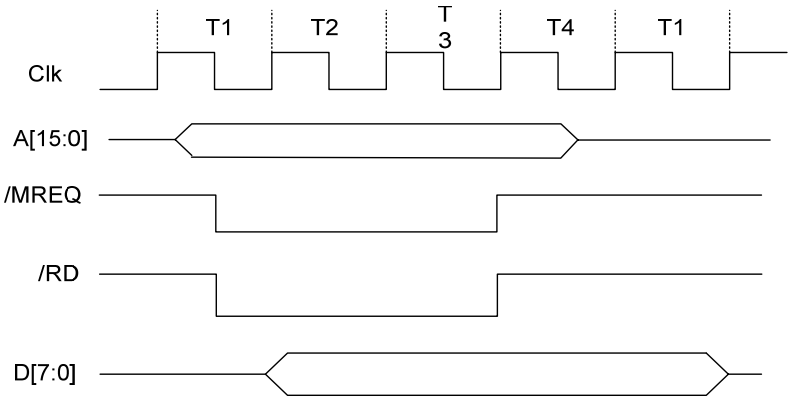
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

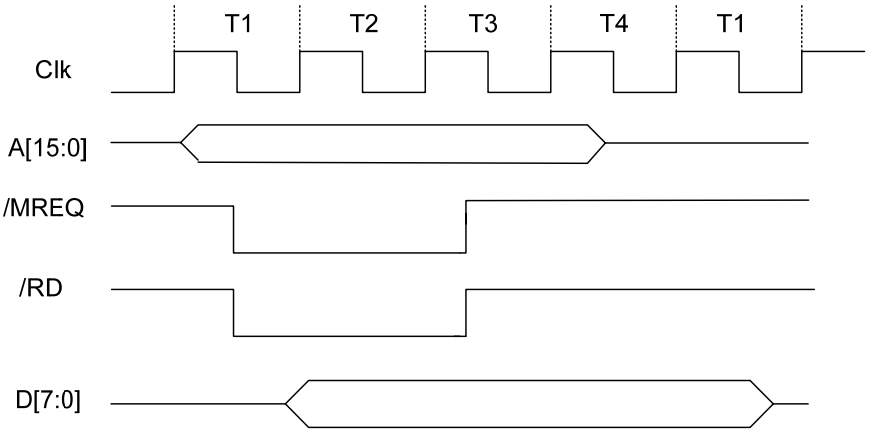
4.11 Bus Operation

Figure 29: Instruction Fetch Timing



Instruction Fetch Timing

Figure 30 Memory Read Timing



Memory Read Timing

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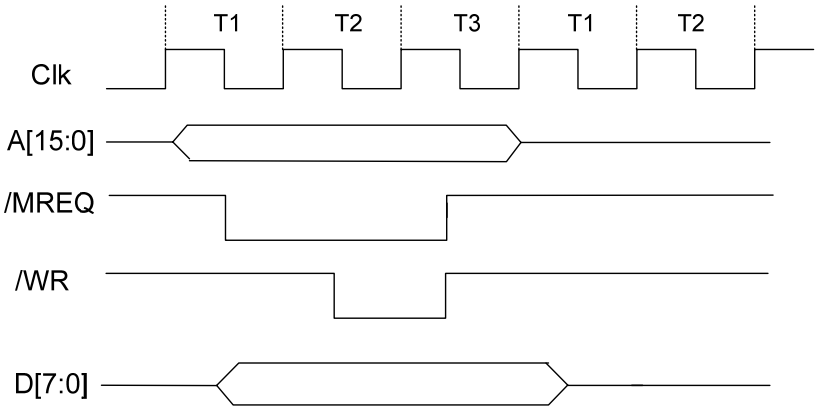
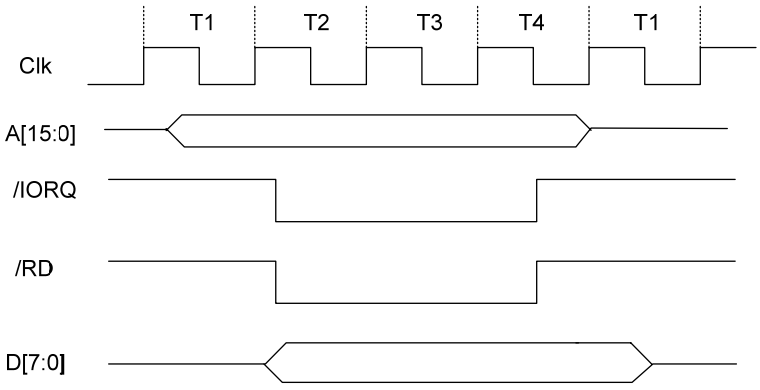
Figure 31: Memory Write Timing



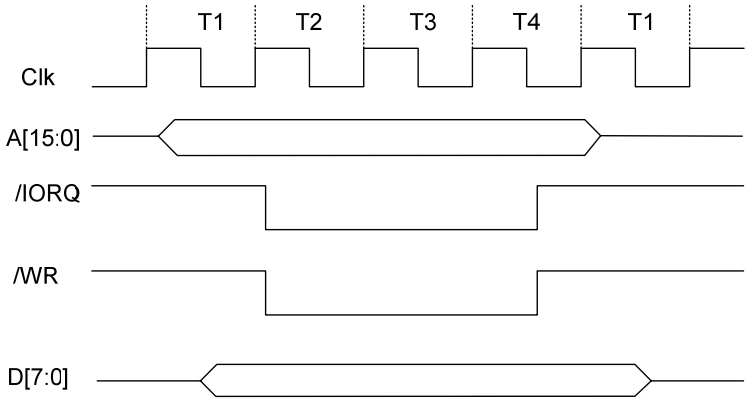
Memory Write Timing

Figure 32: IO Read Timing



IO Read Timing

Figure 33: IO Write Timing



IO Write Timing

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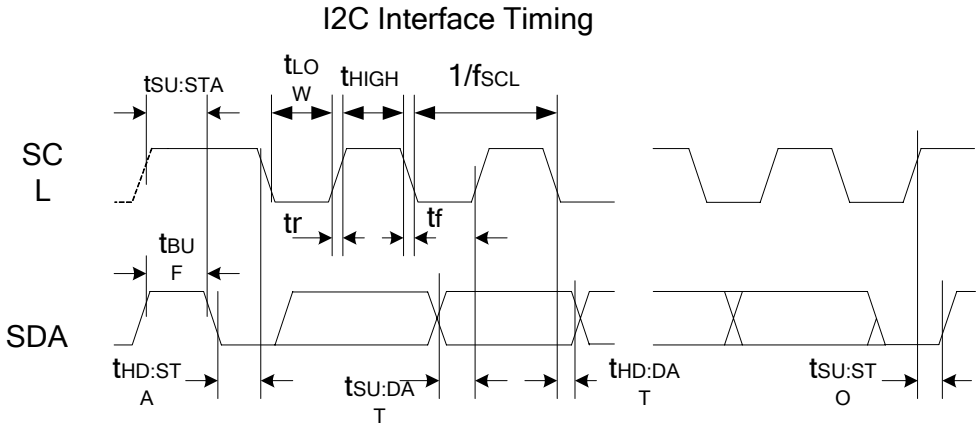
4.12 I2C Interface Parameter

Table 25: I2C Interface Parameter

Parameter	Symbol	Typical		Unit
SCL period	f_{SCL}	100	400	kHz
Clock low time	T_{LOW}	5.0	1.26	us
Clock high time	T_{HIGH}	4.96	1.22	us
Clock rise time	t_r	90	90	ns
Clock fall time	t_f	7.5	8	ns
Data setup time	$t_{SU:DAT}$	3.7	0.68	us
Data hold time	$t_{HD:DAT}$	1.24	0.74	us
Start hold time	$t_{HD:STA}$	9.2	2.45	us
Start setup time	$t_{SU:STA}$	5.3	1.3	us
Stop setup time	$t_{SU:STO}$	5.3	1.3	us

Figure 34: I2C Interface Timing



4.13 A/D Converter Characteristics

Table 26: A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.8 V, VCC = 3.1V, Sample Rate=48KHz)

Characteristics	Min.	Typ.	Max.	Unit

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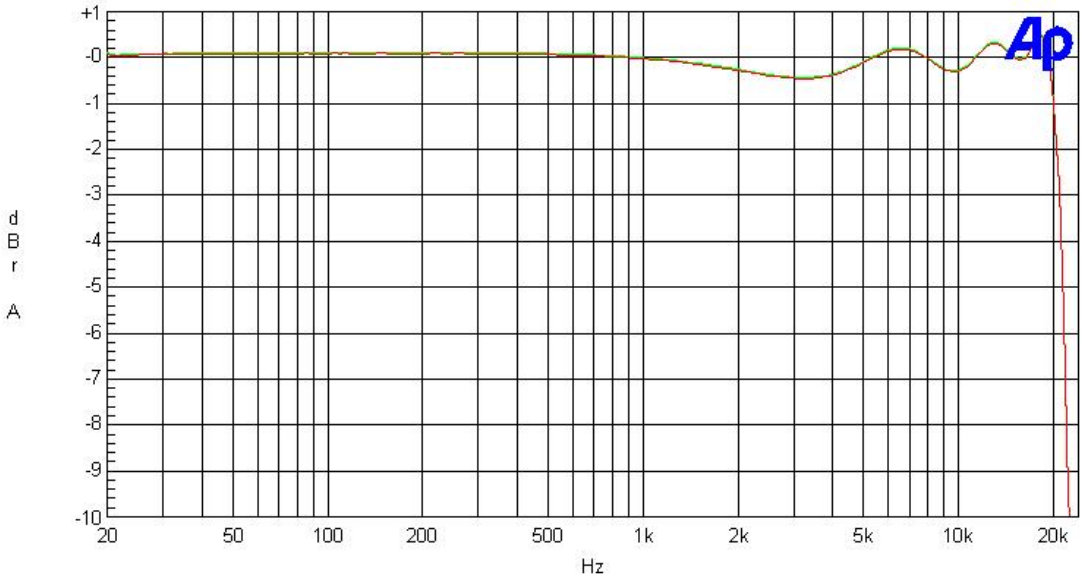
Dynamic Range –40 dBFS Input		89		dB
Total Harmonic Distortion+Noise		-81		dB
Frequency Response 20-18KHz			0.5	dB
Reference Voltage		1.510		V
Full Scale Input Voltage		2.58		Vpp

Figure 35: A/D Converter – Frequency Response Characteristics



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Anlr.Level A	Left	
1	2	Red	Solid	1	Anlr.Level B	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

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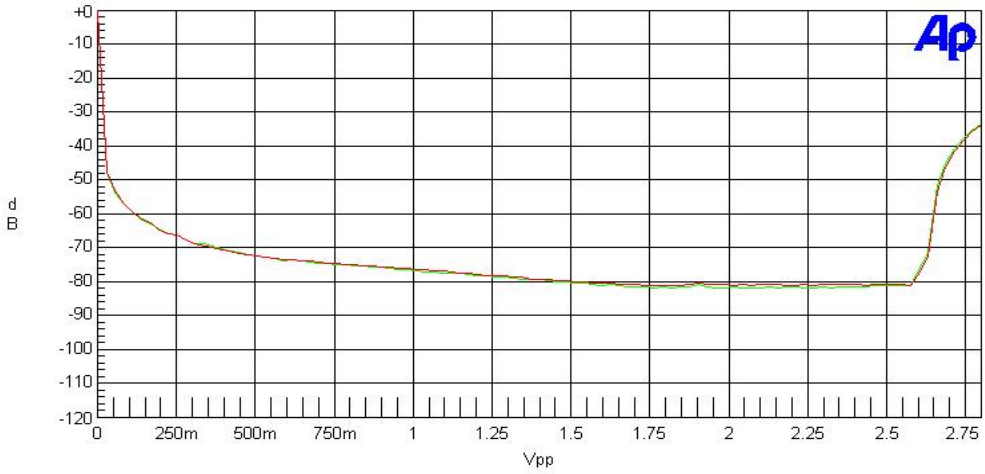
Figure 36: A/D Converter – THD+N vs AMP

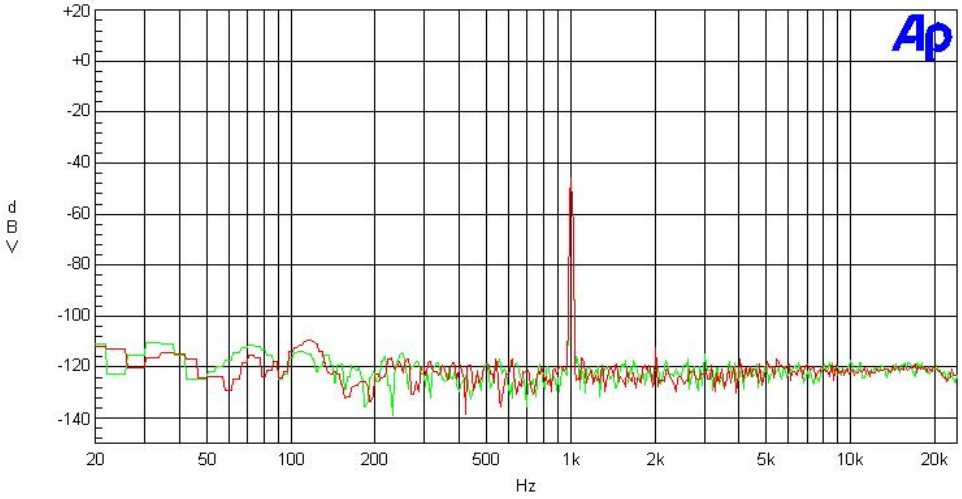


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Red	Solid	1	Anlr.THD+N Ratio	Left	

DSP required. Simultaneous THD+N measurement can be made by using both the Analog Analyzer and the DSP Audio Analyzer in THD+N mode (see pg 1). Filters choice is limited in the DSP Analyzer. Set bandwidth for similar range. At low distortion amplitudes the DSP analyzer is limited by the A-D quantization noise and distortion as can be seen here.

A-A THD+N VS FREQ 2-CH.at27

Figure 37: A/D Converter –Small Signal Power Spectrum



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Red	Solid	1	Fft.Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

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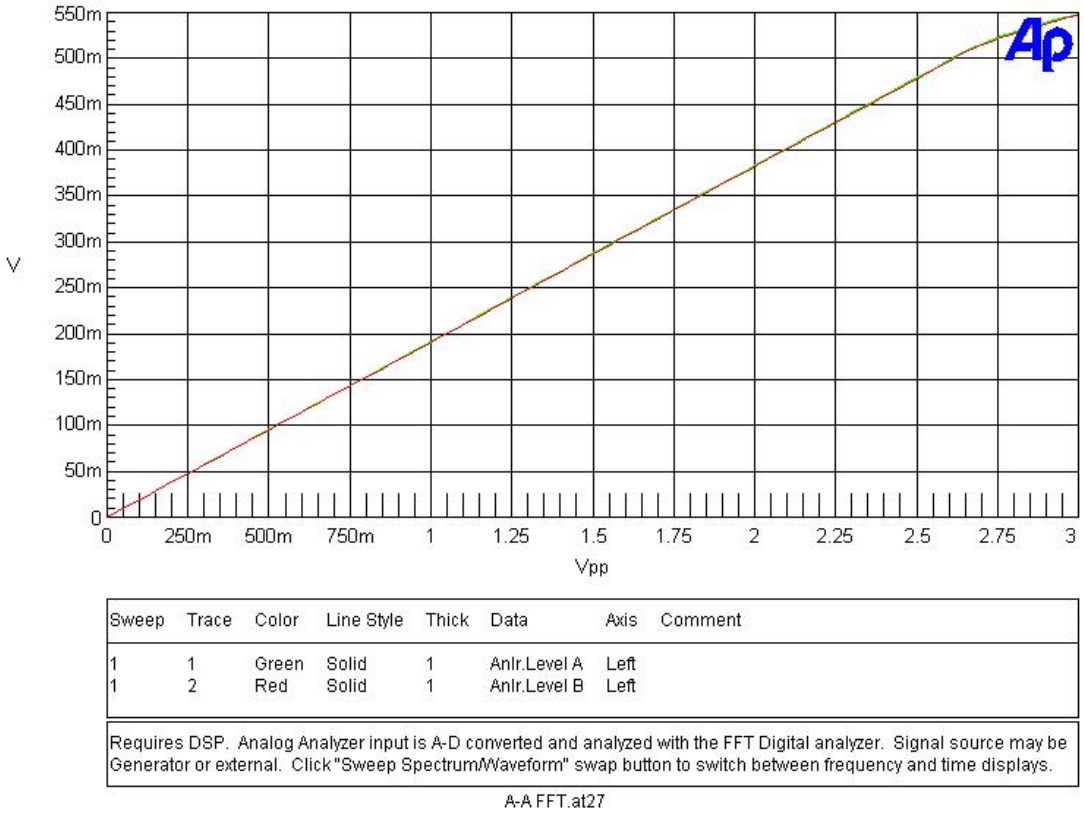
Figure 38: A/D Converter – Linearity



4.14 DAC Characteristics

Table 27: DAC Characteristics

Characteristics	MIN.	Typ.	MAX.	UNIT
Dynamic Range –48 dBFS Input		91.5		dB
Total Harmonic Distortion + Noise		-85.5		dB
Full Scale Output Voltage	0.48	0.58	0.72	Vrms
Interchannel Isolation (1k)		-99/-81		dB

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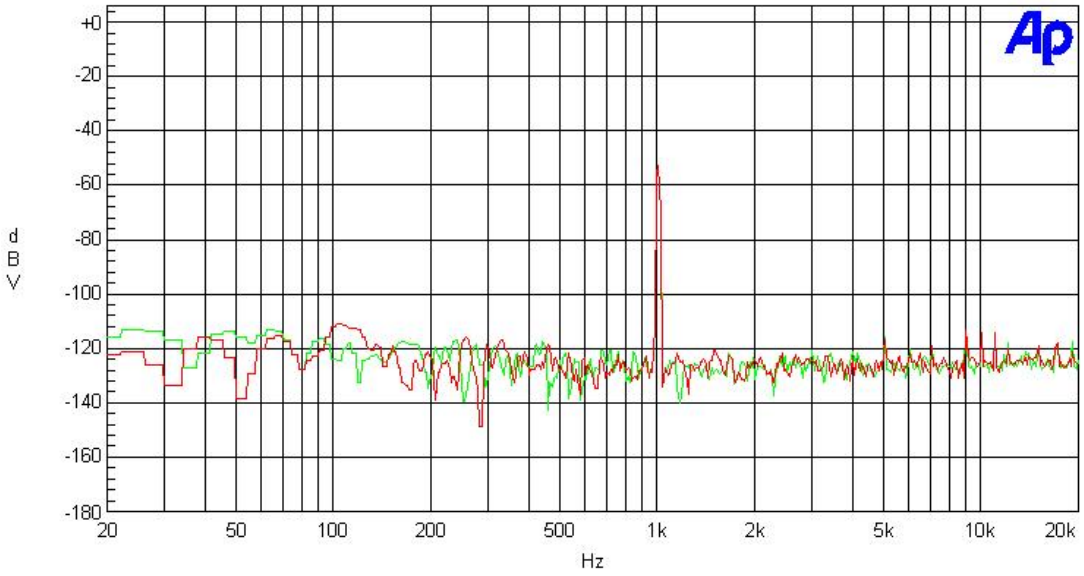
Figure 39: DAC –Small Signal Power Spectrum



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Red	Solid	1	Fft.Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

4.15 Headphone Driver Characteristics

(T_A =-10 - +70℃, VDD = 2.0 V, VCC = 3.0 V, Sample Rate=48KHz, , Volume Level=0x1F)

Table 28: Headphone Driver Characteristics

Characteristics	MIN.	Typ.	MAX.	UNIT
Dynamic Range		94		dB
Total Harmonic Distortion+Noise		-90		dB
Output Common Mode Voltage		1.516		Vrms
Full Scale Output Voltage@-70dB thd+n		1.77		Vpp
Output Power @16ohm		24		mW

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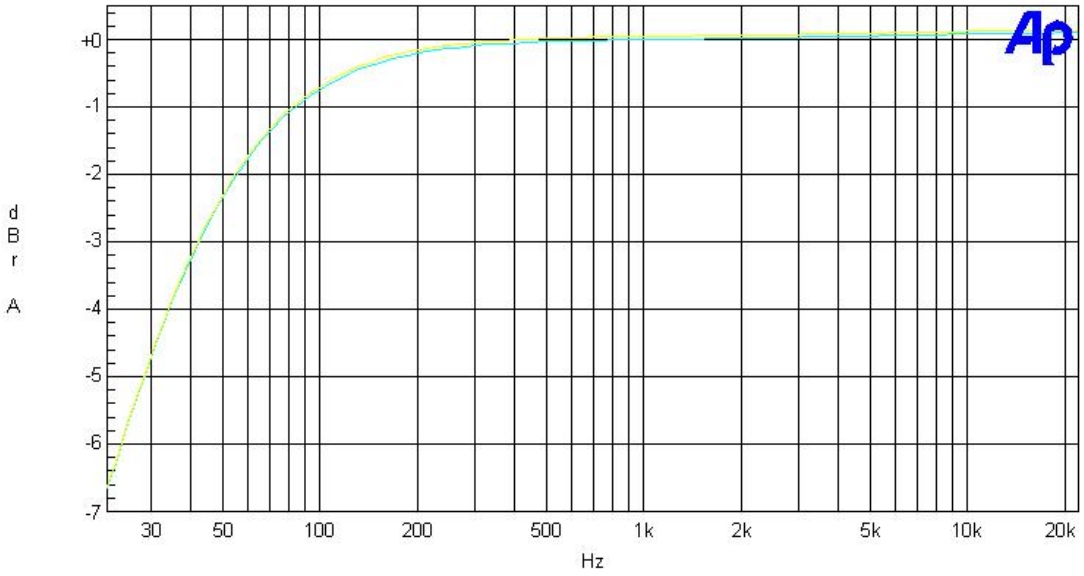
Figure 40: Headphone Driver–Frequency Response



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.Level A	Left	
1	2	Yellow	Solid	1	Anlr.Level B	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

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Figure 41: Headphone Driver–THD + N Amplitude Diagram of Headphone Driver

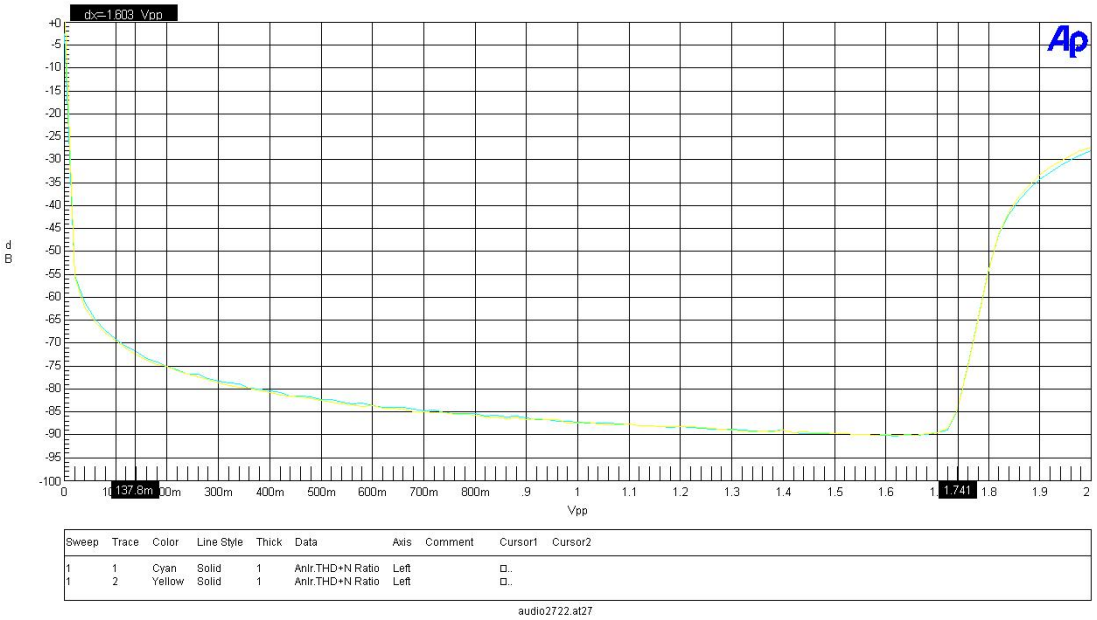

Figure 42: Headphone Driver–Small Signal Power Spectrum

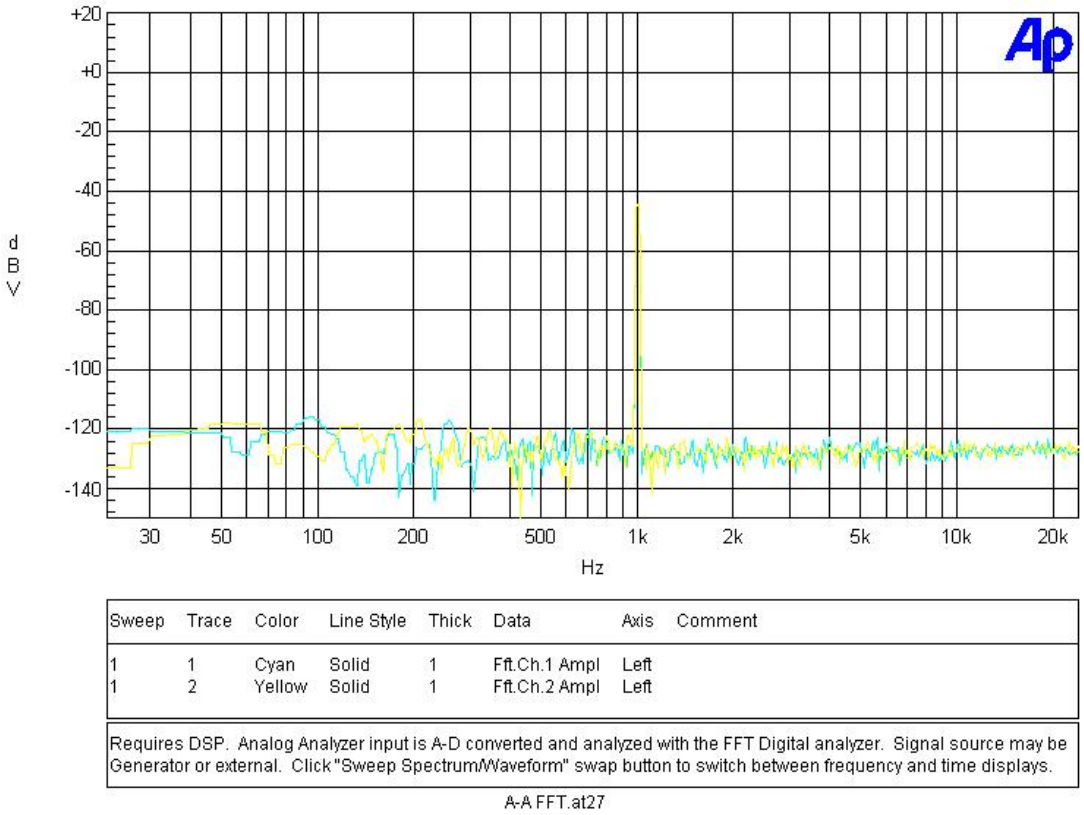

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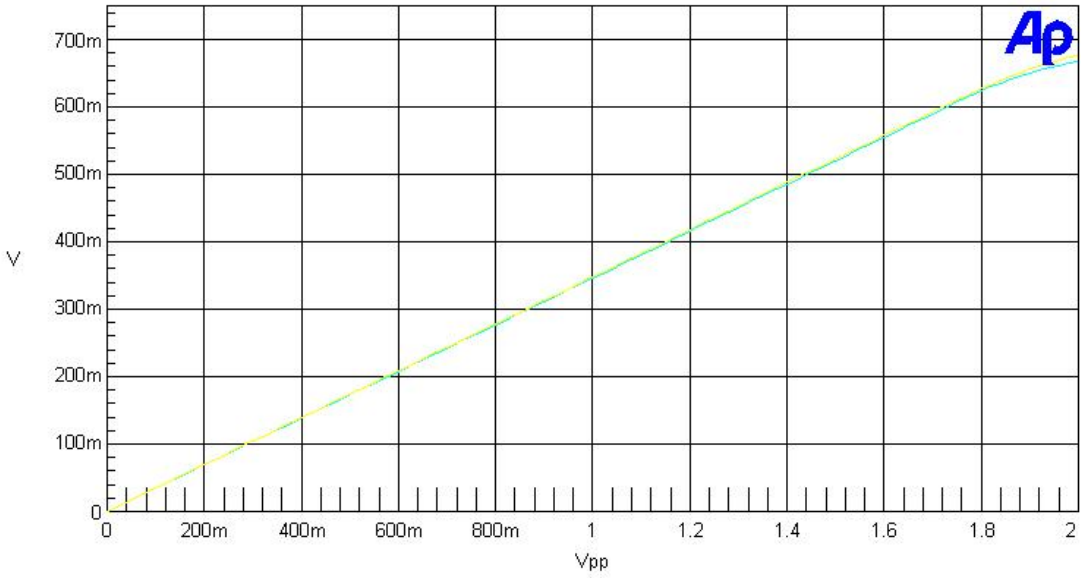
Figure 43: Headphone Driver—Linearity



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.Level A	Left	
1	2	Yellow	Solid	1	Anlr.Level B	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

4.16 LCM Driver Parameter

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Figure 44: LCM Timing

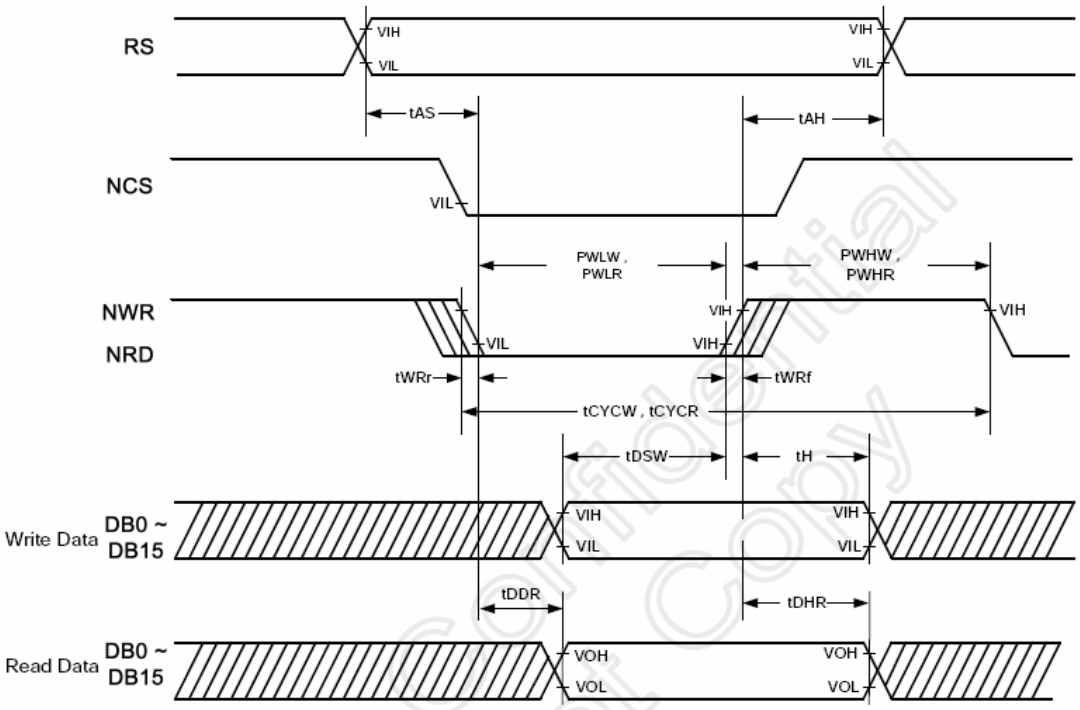

Table 29: LCM Driver Parameter

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	tCYCW	ns	34	200	-	AHB clk.=60MHz
	Read	tCYCR	ns	34	134	-	AHB clk.=60MHz
Write low-level pulse width		PWLW	ns	17	100	-	AHB clk.=60MHz
Read low-level pulse width		PWLR	ns	17	67	-	AHB clk.=60MHz
Write high-level pulse width		PWHW	ns	17	100	-	AHB clk.=60MHz
Read high-level pulse width		PWHR	ns	17	67	-	AHB clk.=60MHz
Write / Read rise / fall time		tWRr , tWRf	ns	-	11	-	AHB clk.=60MHz
Write data set up time		tDSW	ns	27	110	-	AHB clk.=60MHz
Write data hold time		tH	ns	23	28	-	AHB clk.=60MHz
Read data delay time		tDDR	ns	-	45	-	AHB clk.=60MHz
Read data hold time		tDHR	ns	-	105	-	AHB clk.=60MHz

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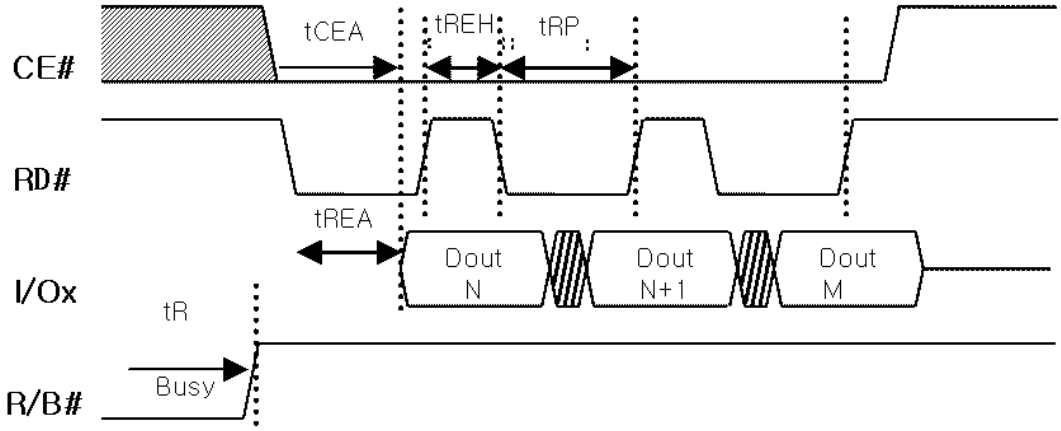
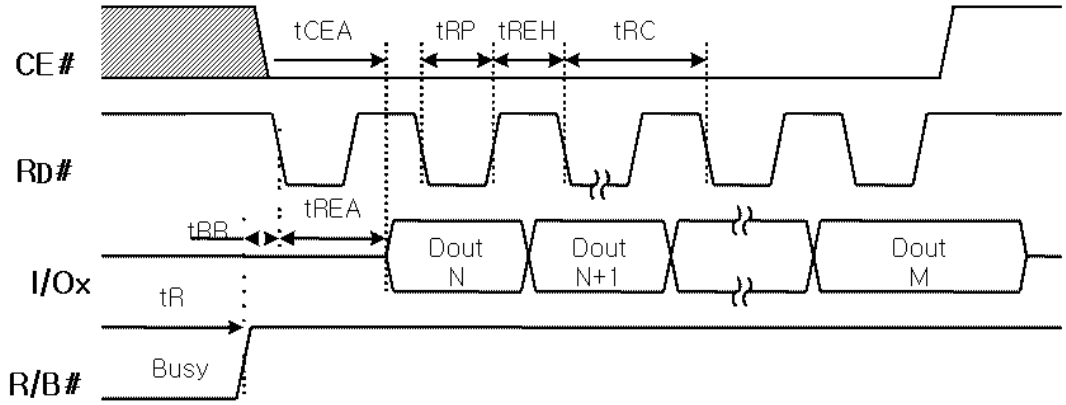
4.17 NAND Flash IF



Data Fetch at RD# Rising Edge

Figure 45: Conventional Serial Access Mode



Data Fetch at RD# Falling Edge

Figure 46: EDO Type Serial Access Mode

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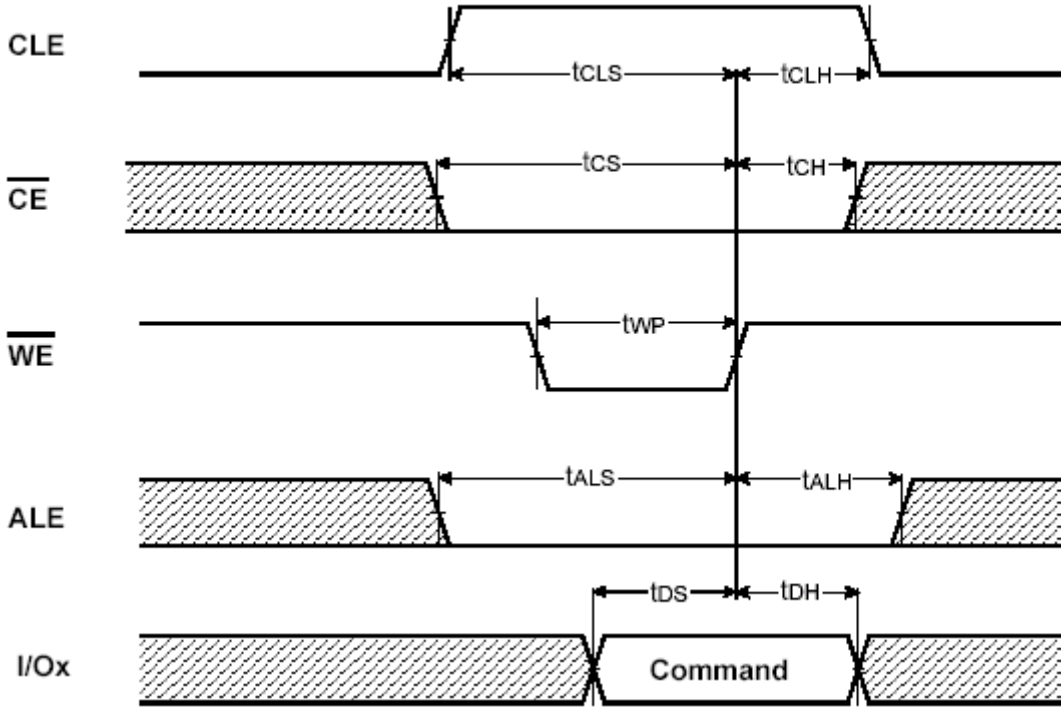
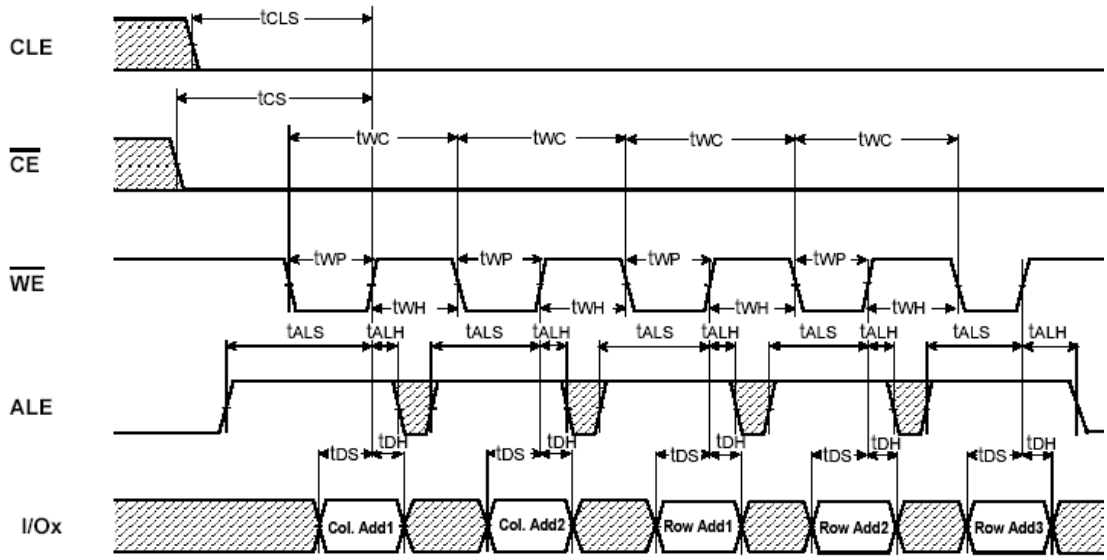
Command Latch Cycle



IO[15:8] must be set to zero

Figure 47: Command Latch Cycle

Address Latch Cycle



IO[15:8] must be set to zero

Figure 48: Address Latch Cycle

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Table 30: Nand Flash Timing Request

Item	Conventional Serial Access	EDO Type Serial Access	Remark
tCEA	23nS (min)	23nS (min)	
tREA	30nS (max)	18nS (max)	
tREH	15nS (min)	12.5nS (min)	
tRP	25nS (min)	12.5nS (min)	
tRC	30nS (min)	25nS (min)	Conventional: duty≠50% EDO type: duty=50%
Data Fetch	At RD# Rising Edge	At next RD# Falling Edge	
tFALLING	5nS	5nS	
tRISINFG	5nS	5nS	
tCLS	25nS (min)	12nS (min)	
tCLH	10nS (min)	5nS (min)	
tCS	35nS (min)	20nS (min)	
tCH	10nS (min)	5nS (min)	
tALS	25nS (min)	12nS (min)	
tALH	10nS (min)	5nS (min)	
tDS	20nS (min)	12nS (min)	
tDH	10nS (min)	5nS (min)	
tWC	30nS (min)	25nS (min)	
DMA clk	30MHz	40MHz	

4.18 SD Card

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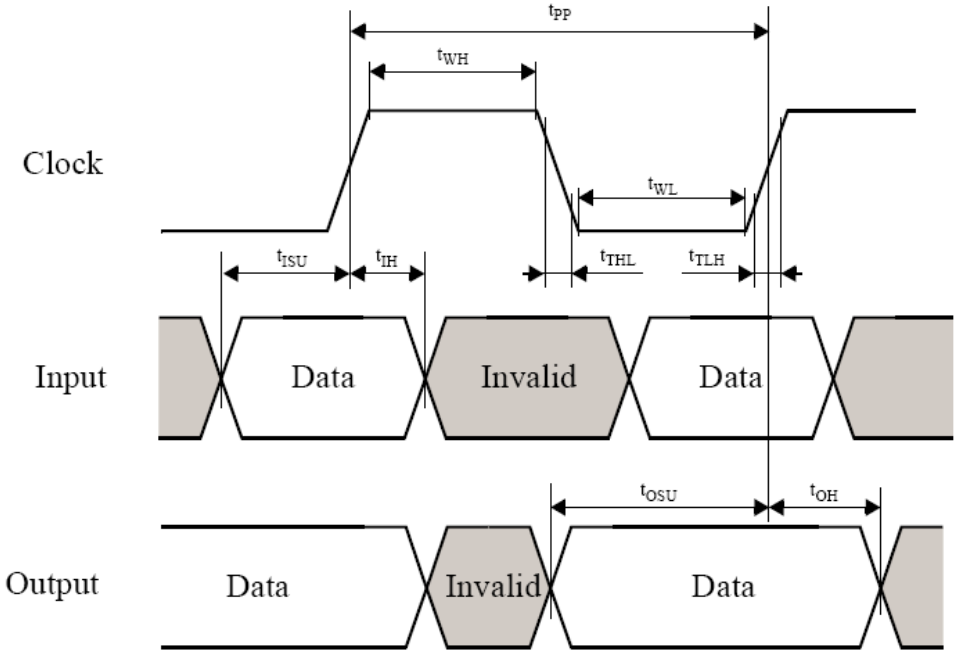

Figure 49: Timing Diagram Data Input/Output Referenced to Clock

Table 31: Card Interface Timings

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	26/52	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open Drain)	fOD	0	400	KHz	Tolerance:+20KHz
Clock low time	tWL	6.5		ns	CL<=30pF
Clock rise time	tTLH		3	ns	CL<=30pF
Clock fall time			3	ns	CL<=30pF
Inputs CMD DAT (reference to CLK)					
Input setup time	tISU	3		ns	CL<=30pF
Input hold time	tIH	3		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	5		ns	CL<=30pF
Output hold time	tOH	5		ns	CL<=30pF
Signal rise time	trise		3	ns	CL<=30pF
Signal fall time	tfall		3	ns	CL<=30pF

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Table 32: Bus Signal Line Load

Parameter	Symbol	Min	Recommend	Max	Unit	Remark
Pull up resistance for CMD	Rcmd	4.7	10	100	KOhm	To prevent bus floating
Pull up resistance for dat0-7	Rdat	50	50	100	KOhm	To prevent bus floating
Bus signal line capacitance	CL			30	pF	Single card
Signal card capacitance	Ccard			7	pF	
Maximum signal line inductance				16	nH	Fpp<=52MHz

CL=CHost+Cbus+Ccard

Table 33: SD Spec. ver1.0 Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock Frequency Data transfer mode	fpp	0	25	MHz	CL<=100Pf
Clock Frequency identification mode	fOD	0~100	400	KHz	CL<=250pF
Clock Low Time	tWL	10		Ns	CL<=100pF
Clock High Time	TWH	10		Ns	CL<=100pF
Clock Rise Time	tTLH		10	Ns	CL<=100pF
Clock Fall Time	tTHL		10	Ns	CL<=100pF
Clock Low Time	tWL	50		Ns	CL<=100pF
Clock High Time	TWH	50		Ns	CL<=100pF
Clock Rise Time	tTLH		50	Ns	CL<=100pF
Clock Fall Time	tTHL		50	Ns	CL<=100pF
Input Set-up Time	tISU	5		Ns	CL<=25pF
Input Hold Time	tIH	5		Ns	CL<=25pF
Output Delay Time under Data Transfer Mode	tODLY		14	Ns	CL<=25pF
Output Delay time under identification transfer mode	tODLY		50	Ns	CL<=25pF

4.19 SDRAM IF

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Figure 50: Standard SDRAM Power Up

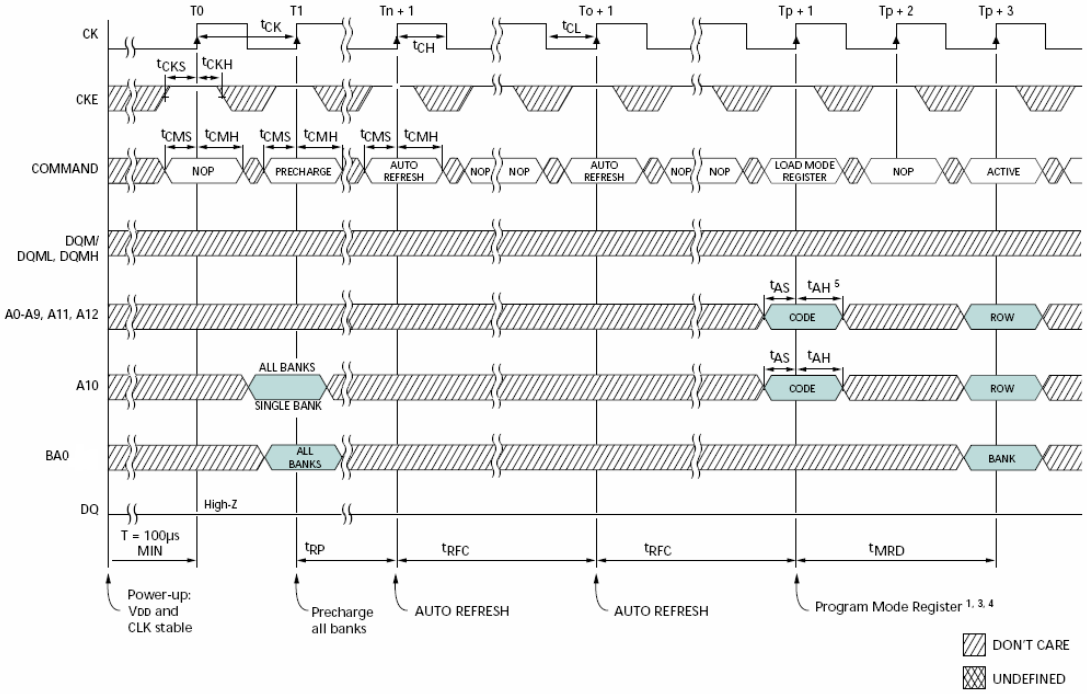
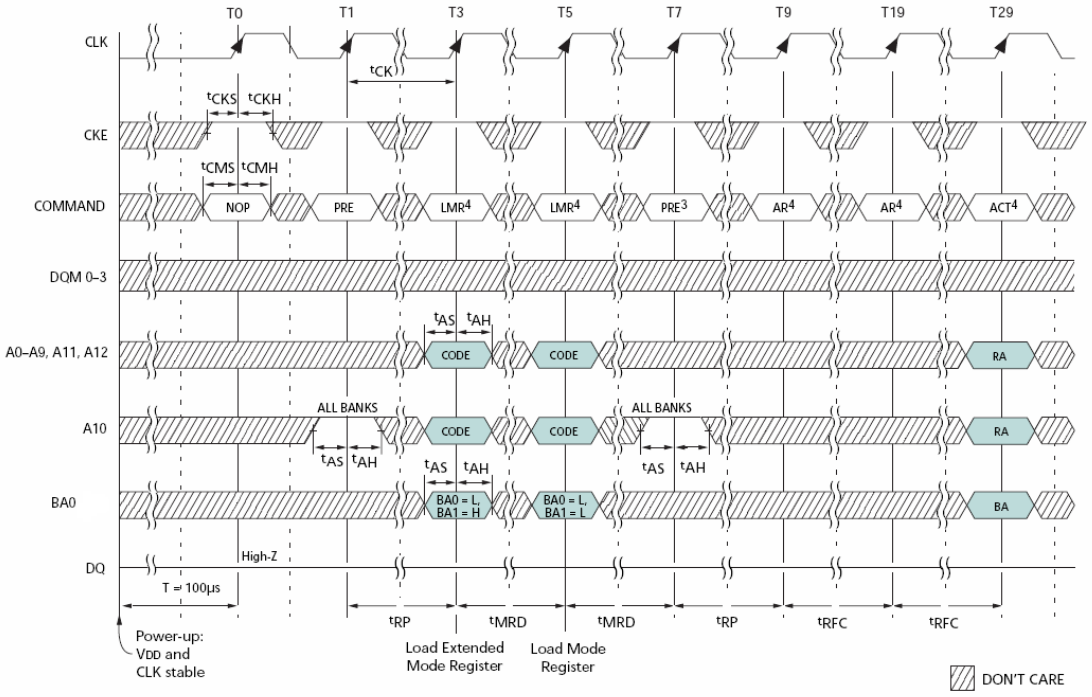


Figure 51: Mobile SDRAM Power Up



NOTE:

1. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
2. If CS is HIGH at clock high time, all commands applied are NOP.

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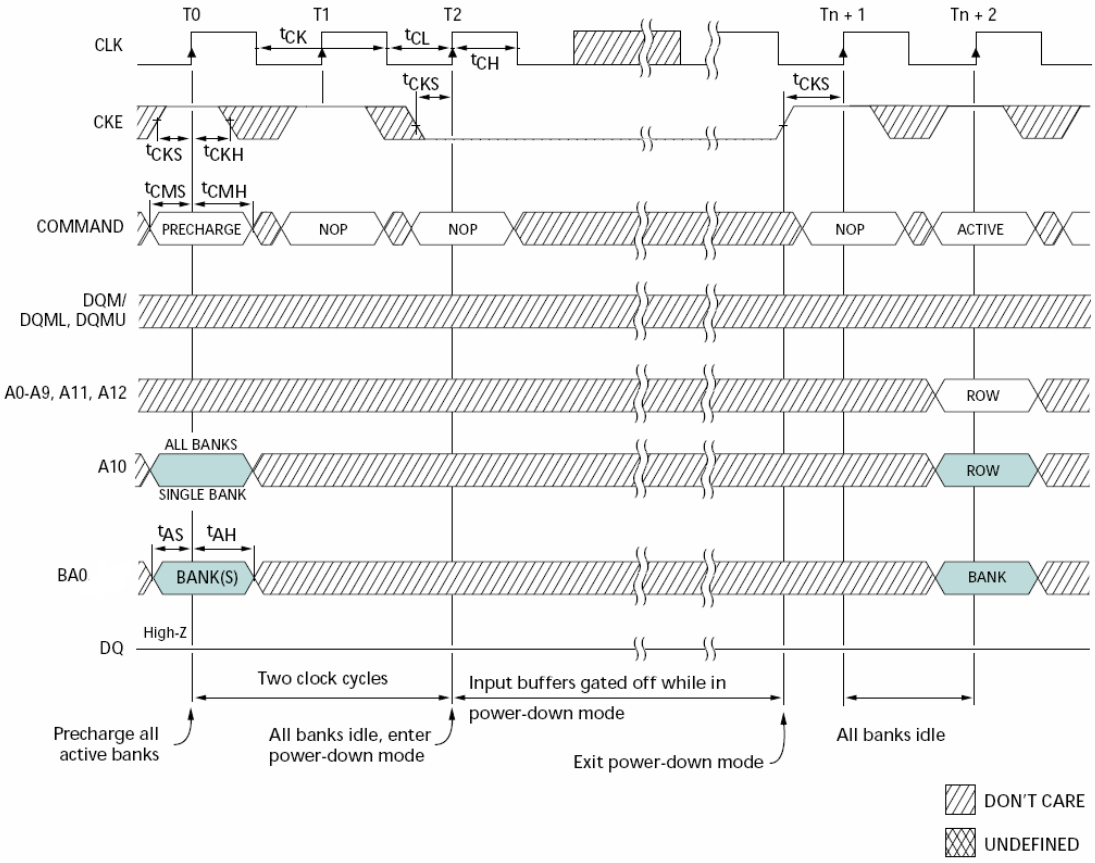
3. Outputs are guaranteed High-Z after command is issued.
4. A12 should be a LOW at tP + 1.

Figure 52: SDRAM IF– Power Down



NOTE:

1. Violating refresh requirements during power-down may result in a loss of data.
2. CAS latency indicated in parentheses

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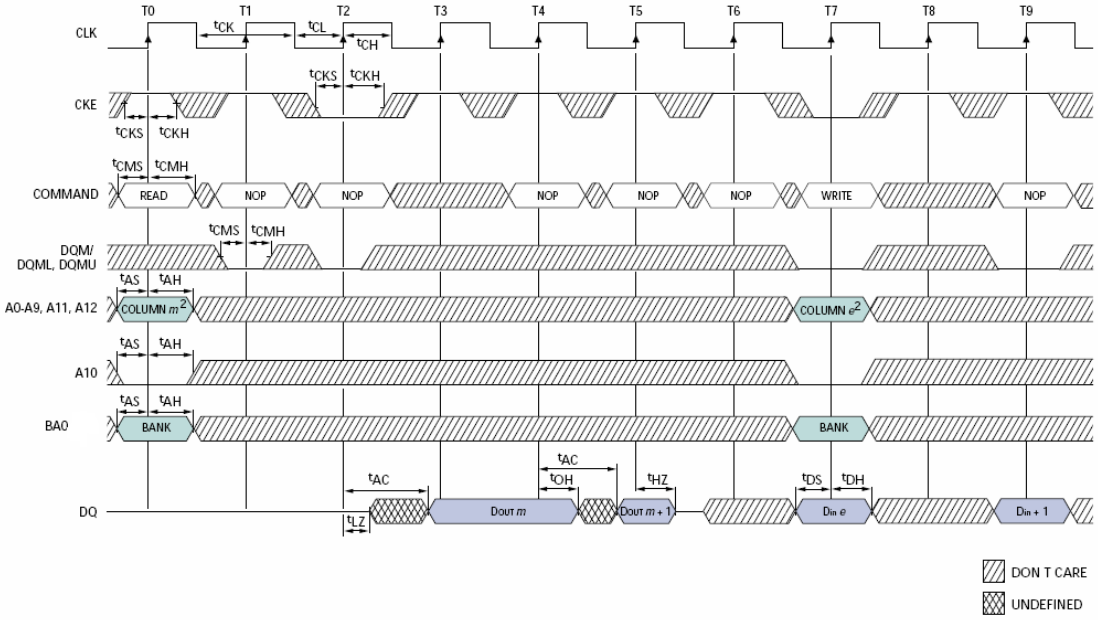
Figure 53: SDRAM IF– Clock Suspend



NOTE:

1. For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.
2. CAS latency indicated in parentheses

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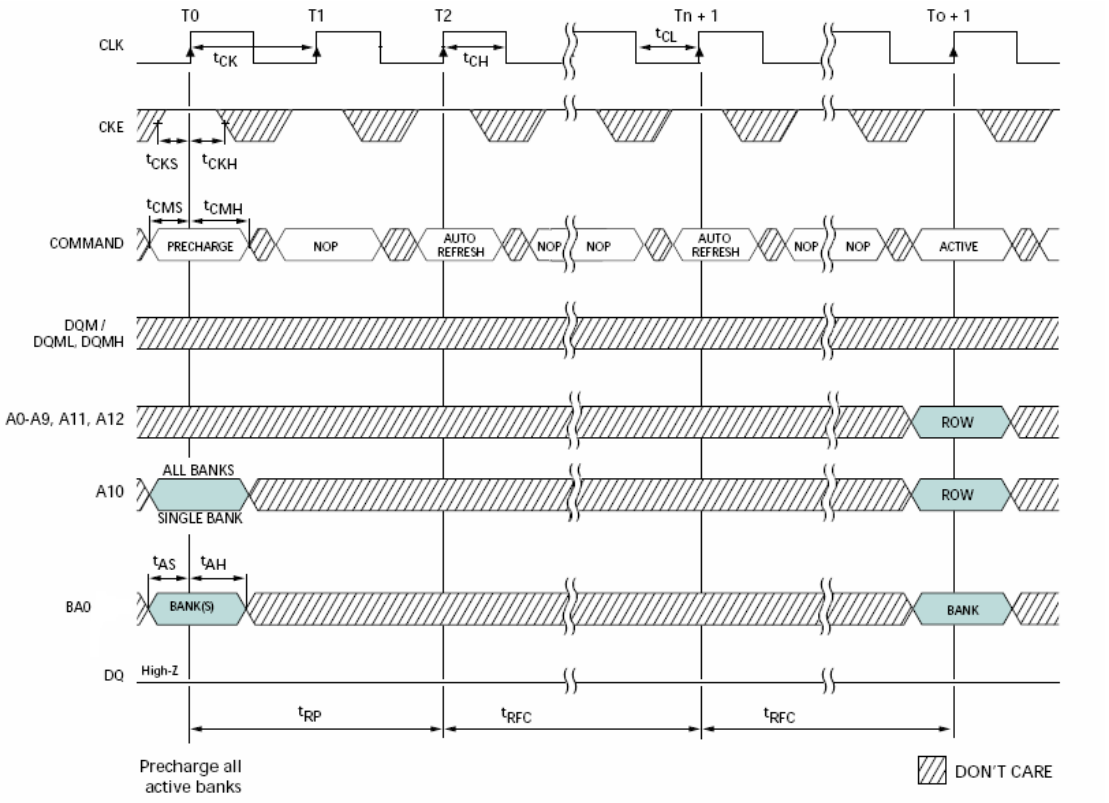
Figure 54: SDRAM IF– Auto Refresh



NOTE:

1. CAS latency indicated in parentheses

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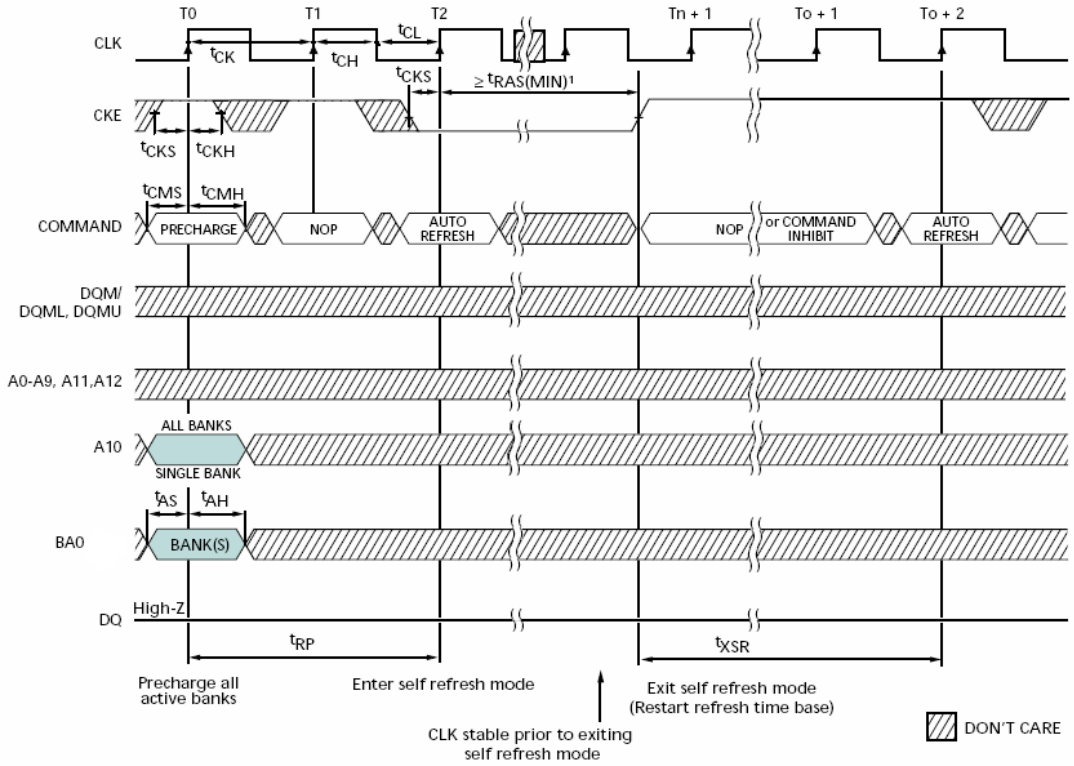
Figure 55: SDRAM IF – Self Refresh



NOTE:

1. No maximum time limit for Self Refresh. tRAS(MIN) applies to non-Self Refresh mode.
2. tXSR requires minimum of two clocks regardless of frequency or timing.
3. CAS latency indicated in parentheses

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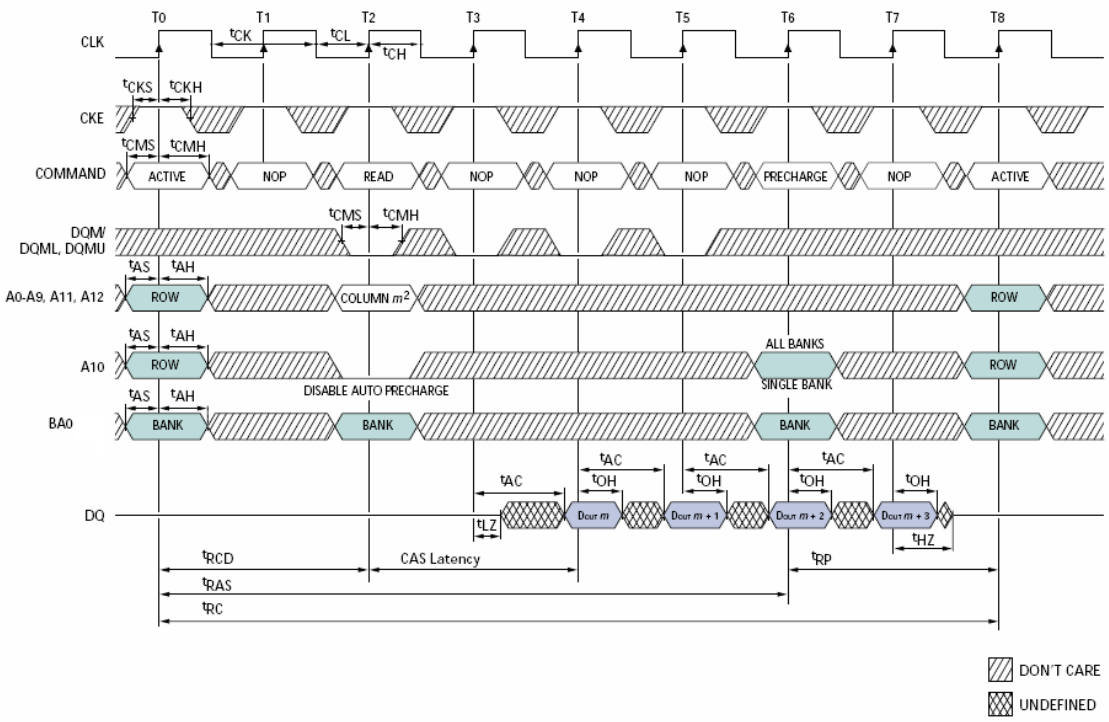
Figure 56: SDRAM IF– Read



NOTE:

1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a “manual” PRECHARGE.
2. CAS latency indicated in parentheses

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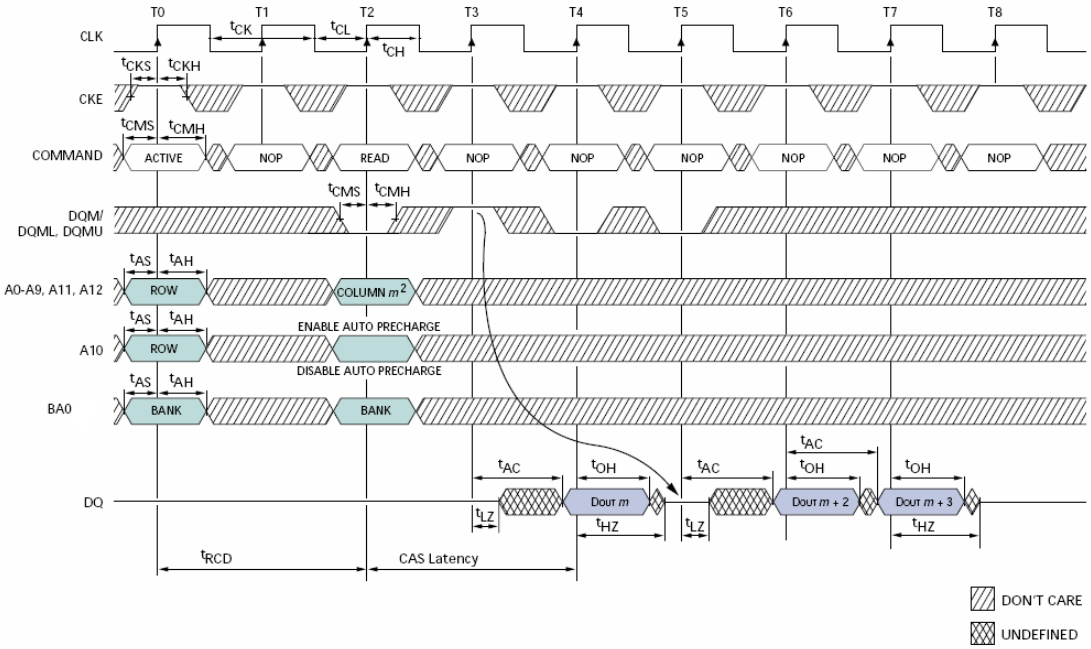
Figure 57: SDRAM IF – Read DQM Operation



NOTE:

1. For this example, the burst length = 4, and the CAS latency = 2.

2. CAS latency indicated in parentheses.

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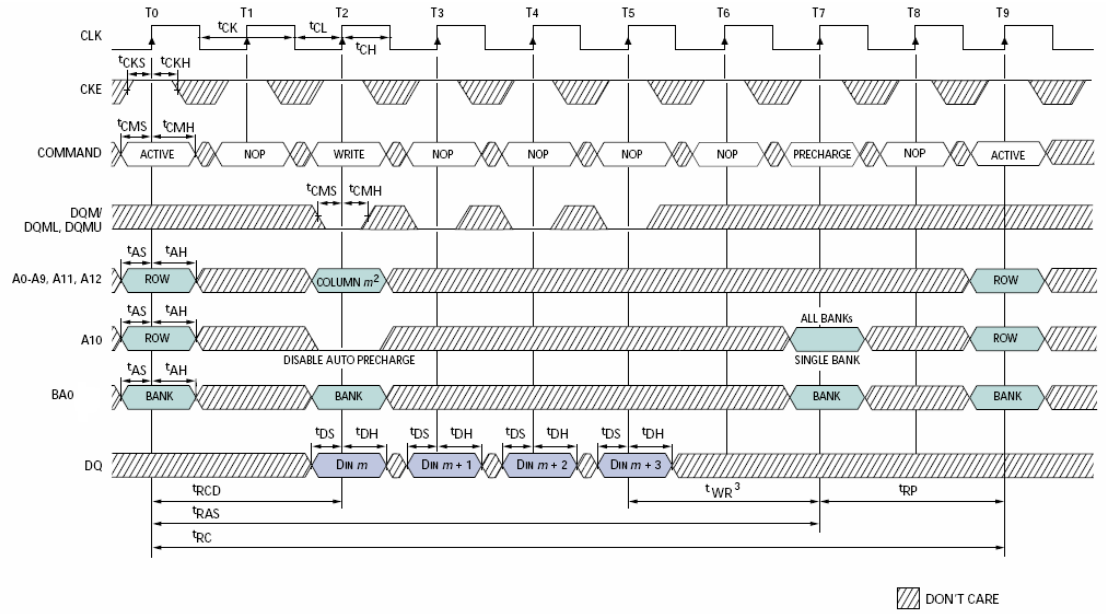
Figure 58: SDRAM IF– Write



NOTE:

1. For this example, the burst length = 4, and the WRITE burst is followed by a “manual” PRECHARGE.
2. 14ns to 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.
3. CAS latency indicated in parentheses.

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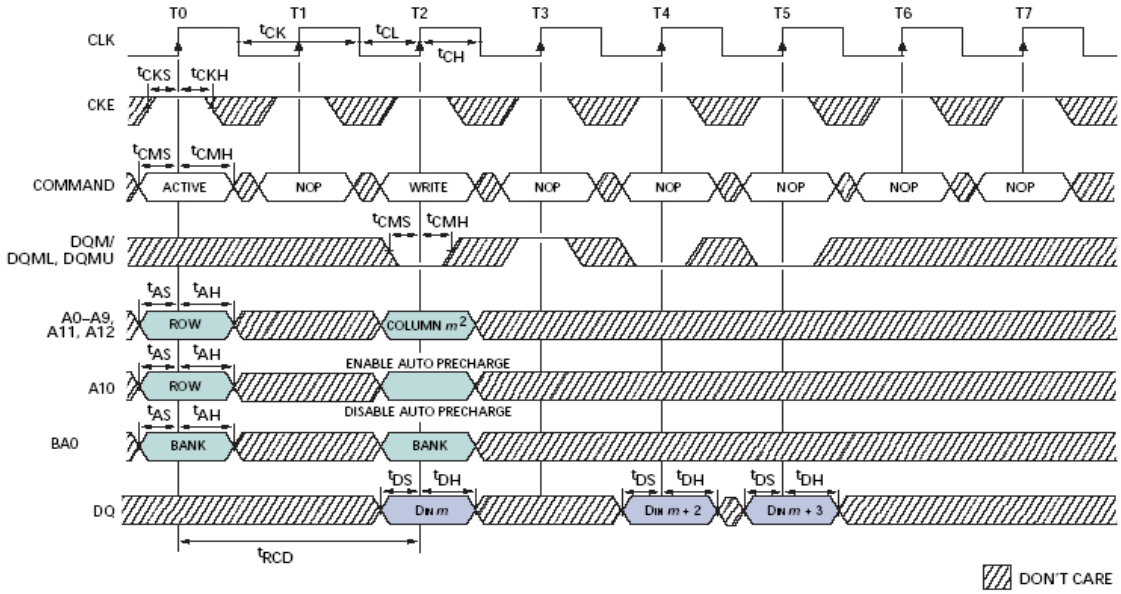
Figure 59: SDRAM IF– Write-DQM Operation



NOTE:

1. For this example, the burst length = 4.
2. CAS latency indicated in parentheses.

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Table 34: SDRAM IF – Parameter

AC Characteristics		Symbol	PC-100		Units
Parameter			Min	Max	
Access time from CLK (positive edge)	CL = 3	tAC (3)		7	ns
	CL = 2	tAC (2)		8	ns
Address hold time		tAH	1		ns
Address setup time		tAS	2.5		ns
CLK high-level width		tCH	3		ns
CLK low-level width		tCL	3		ns
Clock cycle time	CL = 3	tCK (3)	10		ns
	CL = 2	tCK (2)	12		ns
CKE hold time		tCKH	1		ns
CKE setup time		tCKS	2.5		ns
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	1		ns
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	2.5		ns
Data-in hold time		tDH	1		ns
Data-in setup time		tDS	2.5		ns
Data-out High-Z time	CL = 3	tHZ (3)		7	ns
	CL = 2	tHZ (2)		8	ns
Data-out Low-Z time		tLZ	1		ns
Data-out hold time (load)		tOH	2.5		ns
Data-out hold time (no load)		tOHN	1.8		ns
ACTIVE-to-PRECHARGE command		tRAS	50	120,000	ns
ACTIVE-to-ACTIVE command period		tRC	100		ns
ACTIVE-to-READ or WRITE delay		tRCD	20		ns
Refresh period		tREF		64	ms
AUTO REFRESH command period		tRFC	100		ns
PRECHARGE command period		tRP	20		ns
ACTIVE bank a to ACTIVE bank b		tRRD	2		tCK

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command				
Transition time	tT	0.5	1.2	ns
WRITE recovery time Auto precharge mode (a)	tWR (a)	1 CLK +5ns		–
Manual precharge mode (m)	tWR (m)	15		ns
Exit SELF REFRESH to ACTIVE command	tXSR	100		ns

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5 Ordering Information

5.1 Recommended Soldering Conditions

Table 35: Soldering Conditions for Surface-mount Devices

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃or more)—(Lead) or 60 seconds or less (217℃or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

5.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate oxide may occur and then it can ultimately degrade the device operation. Measures must be

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taken to stop the generation of static electricity as many as possible, and it is a must to quickly dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

5.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to the corresponding power SDRVP/VCC etc. or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

5.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

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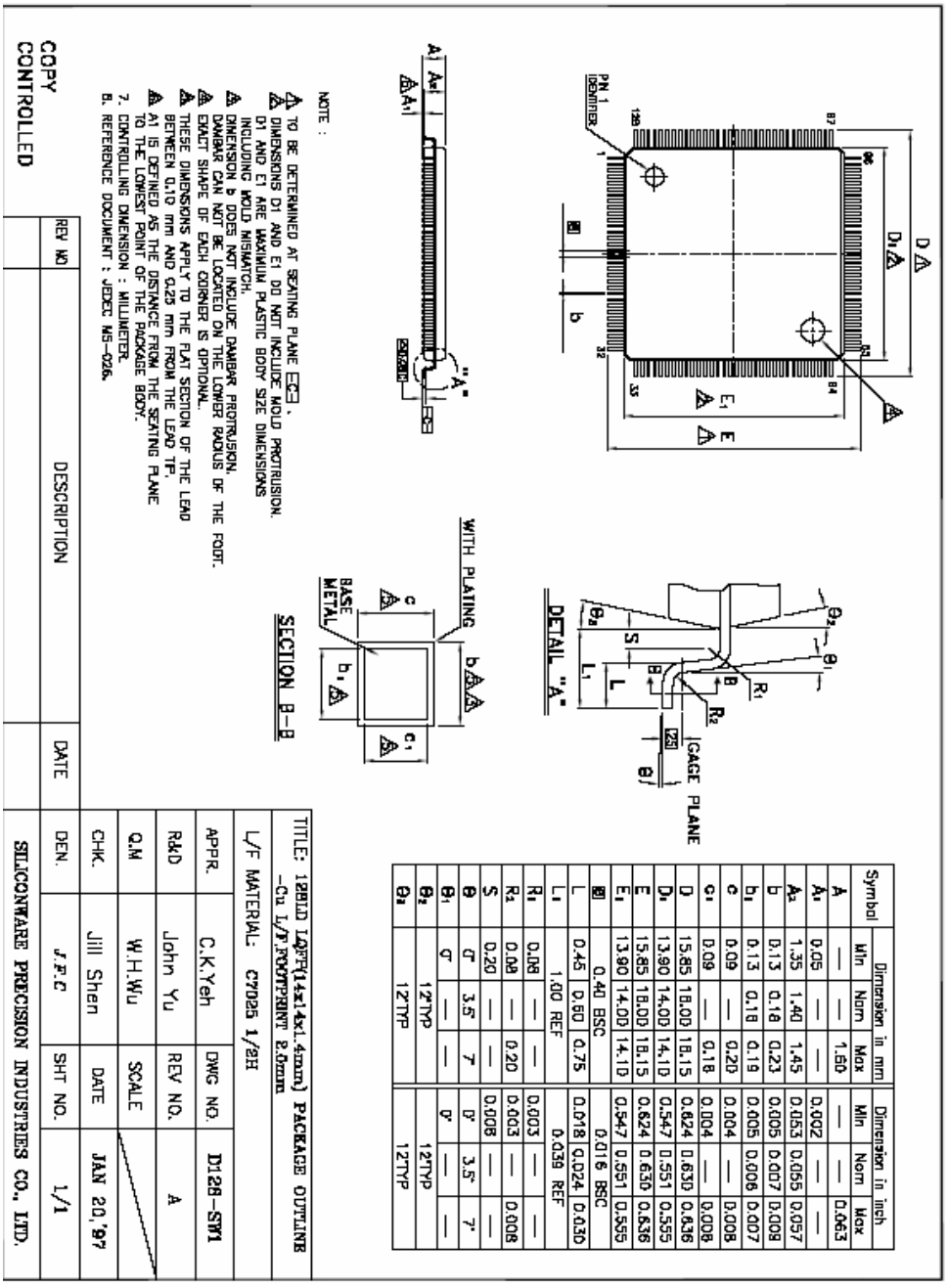
6 ATJ2135N Package Drawing

Figure 60: ATJ2135N Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.18	0.19	0.005	0.008	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.18	0.004	—	0.008
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

REV NO	DESCRIPTION	DATE

COPY CONTROLLED

TITLE: 128LD LQFP(14x14x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

APPR.	C.K.Yeh	DWG NO.	D128-SW1
R&D	John Yu	REV NO.	A
Q.M	W.H.Wu	SCALE	
CHK.	Jill Shen	DATE	JAN 20,'97
DEN.	J.F.C	SHT NO.	1/1

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7 Appendix

7.1 Acronym and Abbreviations

ADC: Analog-to-Digital Converter

AHB: Advanced High-Performance Bus

ALE: Address-Locked Enable

APB: Advanced Peripheral Bus

ATA: Advanced Technology Attachment

BIST: Built-in Self-Test

CLE: Command-Locked Enable

CMU: Clock Management Unit

CP0: System Control Coprocessor

CRC: Cyclic redundancy Check

CVBS: Composite Video Broadcasting Signal

DAC: Digital-to-Analog Converter

dB: Decibel

DC: Direct Current

DSP: Digital Signal Processing

DVB: Digital Video Broadcasting

EAV: End of Active Video

ECC: Error Correct Code

FIR: Fast Infrared

GPIO: General-Purpose Input/Output

I2C: Inter-Integrated Circuit

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I2S: Inter-IC Sound

IR: Infrared

IrDA: Infrared Data Association

IRQ: Interrupt Request

JPEG: Joint Photographic Experts Group

Li-Ion: Lithium Ion (battery type)

LRADC: Low Resolution ADC

MAC: Multiplier Accumulator Control

MCA: Motion Compensation Accelerator

MHA: Media Hardware Accelerator

MIPS: Million Instructions Per Second

MIR: Mid Infrared

MJPEG: Motion JPEG

MMC: Multimedia Card

MMU: Memory Management Unit

MLC: Multi-Level Cell

MPEG: Motion Picture Expert Group

NTSC: National Television Standards Committee

OLED: Polymer Light-Emitting Diode

OTG: On the Go

PA: Power Amplifier

PAL: Phase Alteration Line

PCM: Pulse Code Modulation

PFM: Pulse Frequency Modulation

PLL: Phase-Locked Loop

PMU: Power Management Unit

PWM: Pulse Width Modulation

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RISC: Reduced Instruction Set Computing

RTC: Real-Time Clock

SAV: Start of Active Video

SD: Secure Digital memory card

SIR: Slow Infrared

SMC: State Machine Controller

SLC: Single-Level Cell

SOC: System on a Chip

SPEC: Specification

SPDIF: SONY-Philips Digital Interface Format

SPI: Serial Peripheral Interface

SPRAM: Scratch Pad RAM

SW: Software

THD: Total Harmonic Distortion

TLB: Translation Look-aside Buffer

TS: Transport Stream

UART: Universal Asynchronous Receiver Transmitter

WMA: Windows Media Audio

WMV: Windows Media Video

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